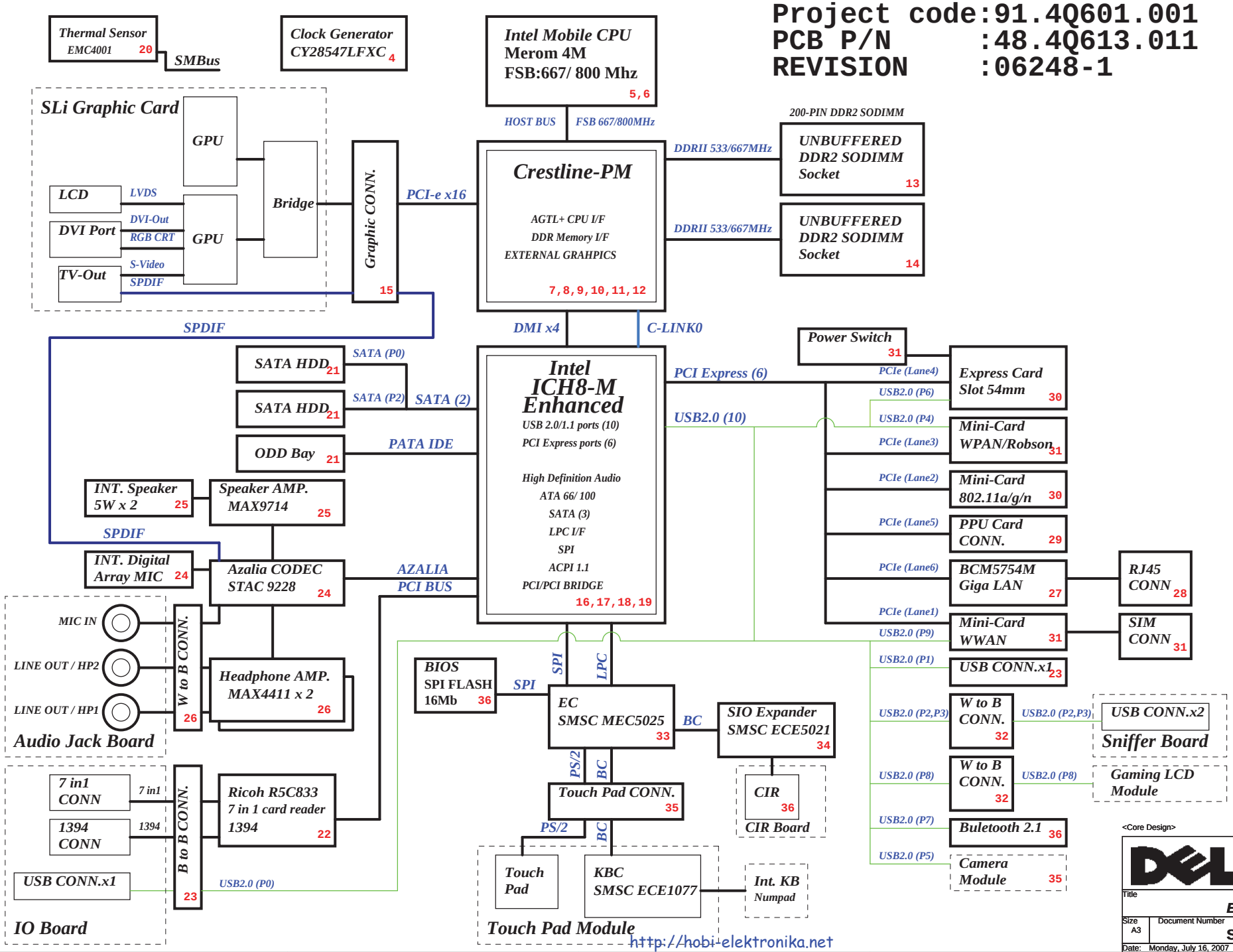
Siberia Block Diagram

Project code:91.4Q601.001
PCB P/N :48.4Q613.011
REVISION :06248-1



System DC/DC TPS51120 46	
INPUTS	OUTPUTS
+PWR_SRC	+5V_ALW +5V_SUS +3.3V_SUS +3.3V_RTC_LDO

System DC/DC SN0508073 44	
+PWR_SRC	+1.5V_RUN +1.25V_RUN

DDR2 DC/DC SN0508073 45	
+PWR_SRC	+1.8V_SUS +1.05V_VCCP

LDO TPS51100 47	
+1.8V_SUS	+0.9V_DDR_VTT

LDO MAX668 47	
+PWR_SRC	+12V_S

Battery Charger ISL88731 41	
INPUTS	OUTPUTS
+PWR_SRC	+VCHGR

CPU DC/DC ISL6260C 42,43	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

PCB LAYER

L1:TOP
L2:GND
L3:Signal
L4:Signal
L5:VCC
L6:Signal
L7:GND
L8:BOT

<Core Design>

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Title: BLOCK DIAGRAM

Size: A3 | Document Number: Siberia | Rev: A00

Date: Monday, July 16, 2007 | Sheet 1 of 50

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CLOCK GEN CY28547

27M_SS/LCD96_100M SELECTION TABLE

BYTE 10

Bit5 S1	Bit4 S0	Spread Spectrum S[1:0]
0	0	-0.5%(Default)
0	1	-1.0%
1	0	-1.5%
1	1	-2.0%

BYTE 15
IO_VOUT[2,1,0]

Bit2 IO_VOUT2	Bit1 IO_VOUT1	Bit0 IO_VOUT0	IO_VOUT[2,1,0]
0	0	0	0.3V
0	0	1	0.4V
0	1	0	0.5V
0	1	1	0.6V
1	0	0	0.7V
1	0	1	0.8V(Default)
1	1	0	0.9V
1	1	1	1.0V

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4 ★
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes number in order) ★
CFG 16 FSB Dynamic ODT	Disabled	Enabled ★
CFG 19 DMI Lane Reserved	Normal Operation ★	Lane Reserved
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation ★	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA SDVO Present	NO SDVO Card Present ★	SDVO Card Present

CFG 12 CFG 13	XOR/ALL-Z
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation

PCIE Routing

LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	BT/UWB/Robson
LANE4	Express Card
LANE5	PPU card
LANE6	Giba Bit LOM

PCI ROUTING

	IDSEL	INT	REQ	GNT
1394/ MediaCard	AD17	C D	1	1

USB TABLE

ICH

USB0	Ext Lift Side
USB1	Ext Back
USB2	Ext Right Side (Top)
USB3	Ext Right Side (Bottom)
USB4	3rd mini card
USB5	Camera
USB6	Express Card
USB7	BT
USB8	Gaming LCD
USB9	WWAN

INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved. Rising Edge of PWROK.	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overidden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap

ICH_RSVD tp3	AZ_DOUT_ICH	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(default)
1	1	Set PCIE port cofig bit1

A16 swap override strap

PCI_GNT#3	
	low = A16 swap override enable
	high = default

BOOT BIOS Strap

PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

integrated VccSus1_05,VccSus1_5,VccCL1_5

SM_INTVRMEN	High=Enable	Low=Disable

integrated VccLan1_05VccCL1_05

LAN100_SLP	High=Enable	Low=Disable

DEFAULE HIGH

No Reboot Strap

SPKR	LOW = Defaule
	High=No Reboot

8.2K PULL HIGH

INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST0#	PULL-UP 13K

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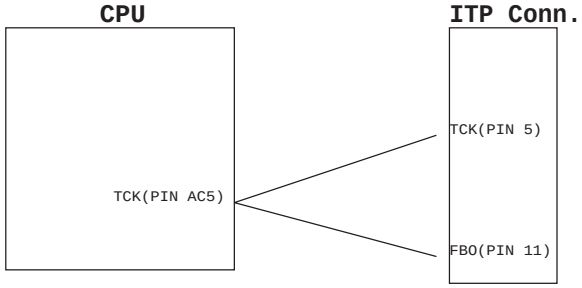

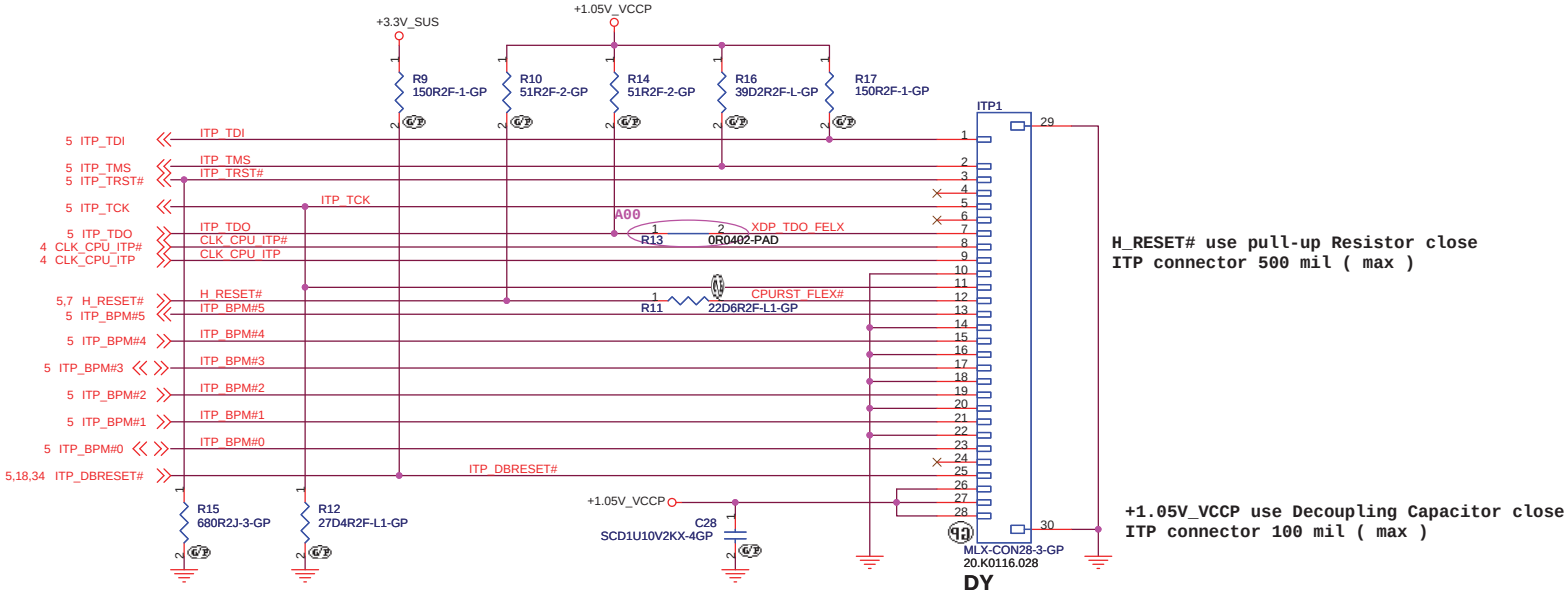

ITP Debug Conn.

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Title	*ITP Debug*	
Size A3	Document Number **Siberia**	Rev **A00**
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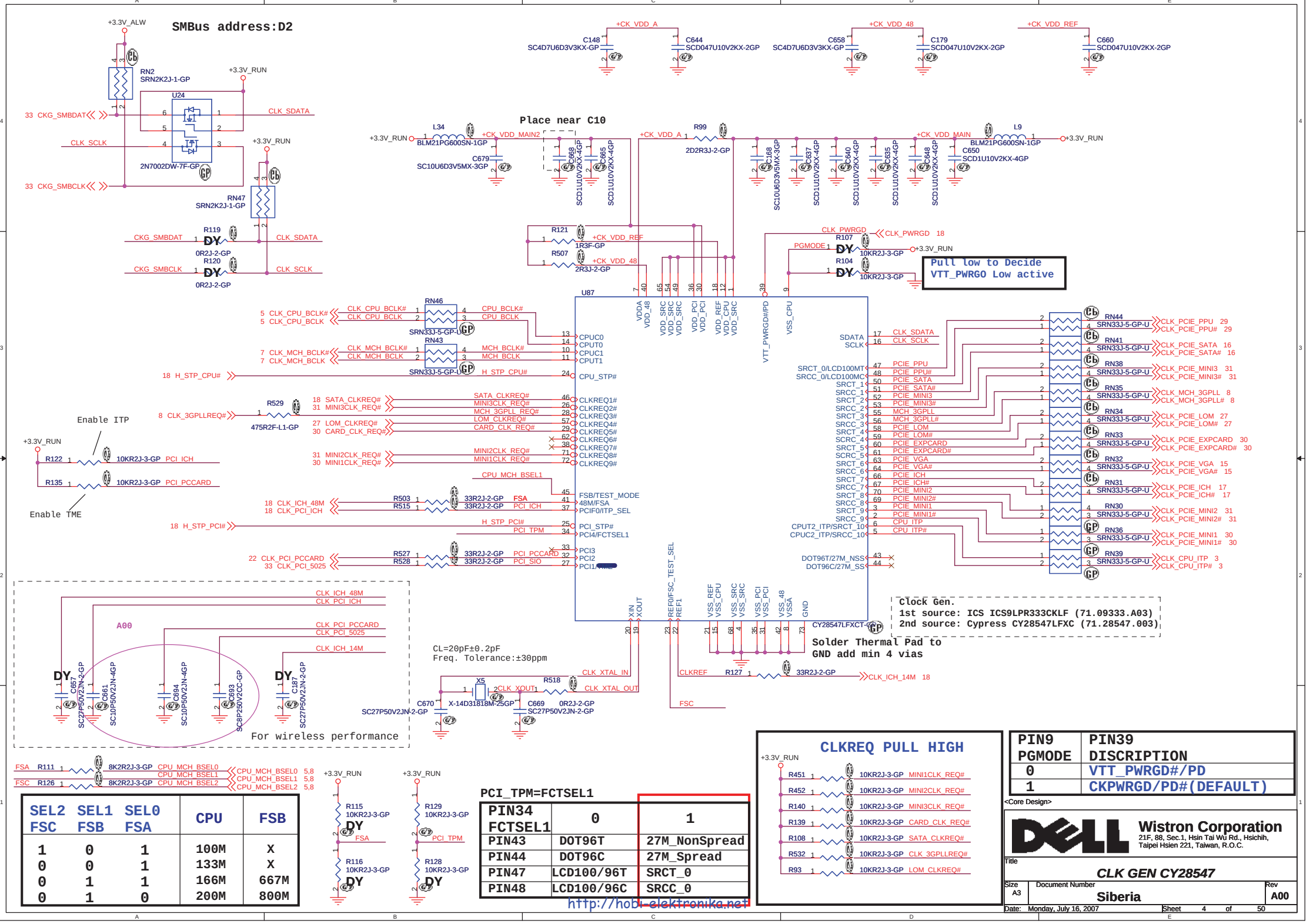
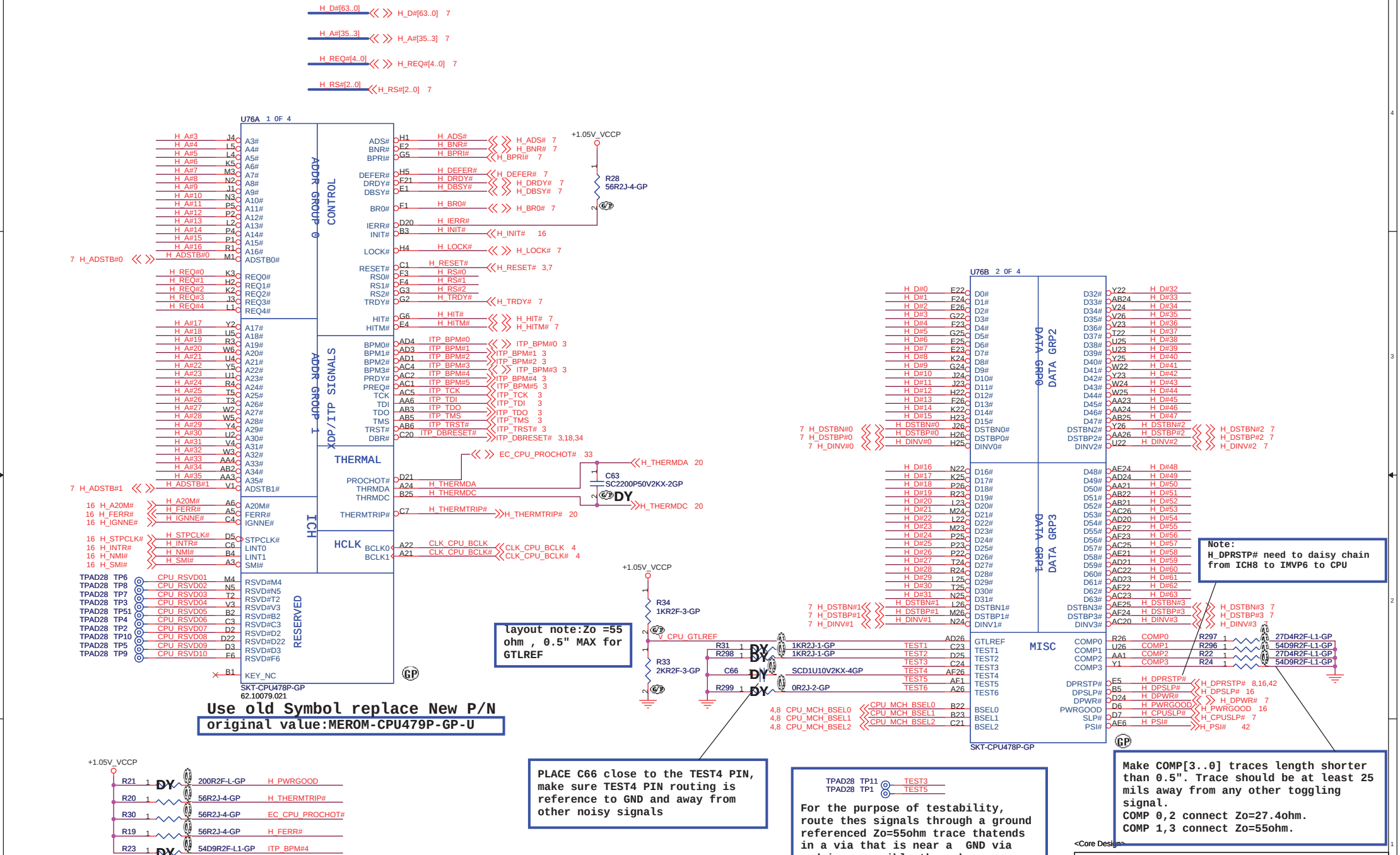


SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

PIN34 FCTSEL1	0	1
PIN43	DOT96T	27M_NonSpread
PIN44	DOT96C	27M_Spread
PIN47	LCD100/96T	SRCT_0
PIN48	LCD100/96C	SRCC_0

PIN9 PGMODE	PIN39 DISCRIPTION
0	VTT_PWRGD#/PD
1	CKPWRGD/PD#(DEFAULT)

<Core Design>



Use old Symbol replace New P/N

original value:MEROM-CPU479P-GP-U

layout note:Zo =55 ohm , 0.5" MAX for GTLREF

PLACE C66 close to the TEST4 PIN, make sure TEST4 PIN routing is reference to GND and away from other noisy signals

For the purpose of testability, route thes signals through a ground referenced Zo=55ohm trace thatends in a via that is near a GND via and is accessible through an oscilloscope connection.

Note:
H_DPRSTP# need to daisy chain from ICH8 to IMVP6 to CPU

Make COMP[3..0] traces length shorter than 0.5". Trace should be at least 25 mils away from any other toggling signal.
COMP 0,2 connect Zo=27.4ohm.
COMP 1,3 connect Zo=55ohm.

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Title: CPU-FSB (1/2)

Size: A3 | Document Number: Siberia | Rev: A00

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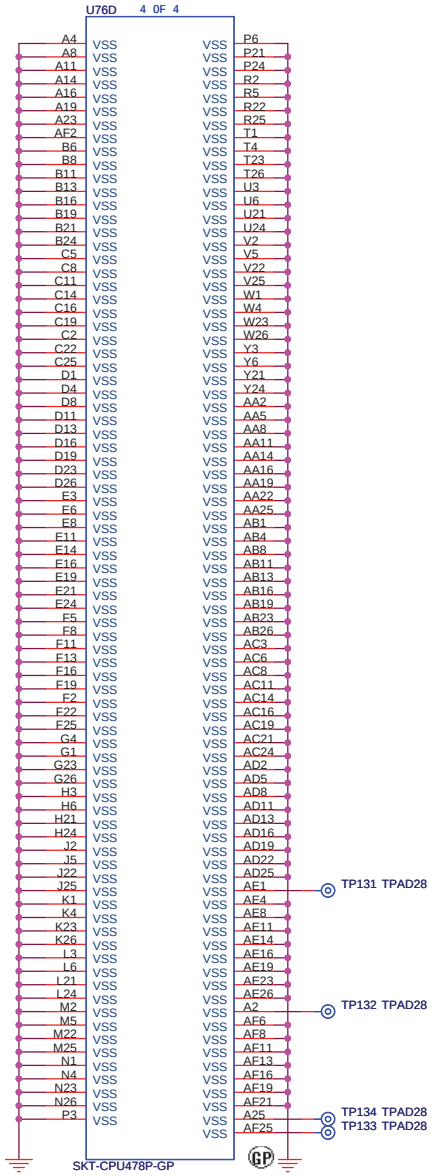

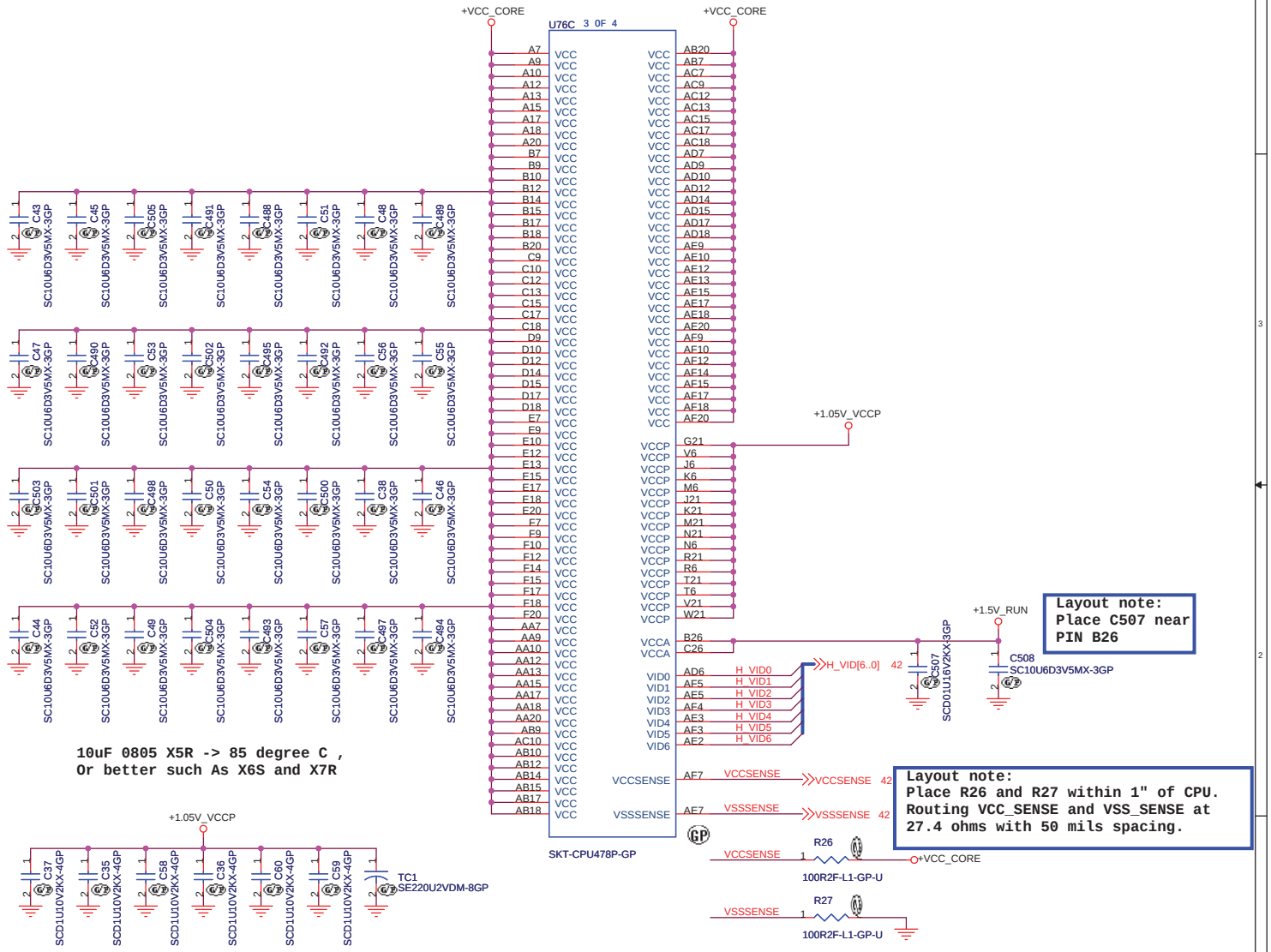

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Title: ***CPU-POWER (2/2)***

Size	Document Number	Rev
A3	**Siberia**	**A00**

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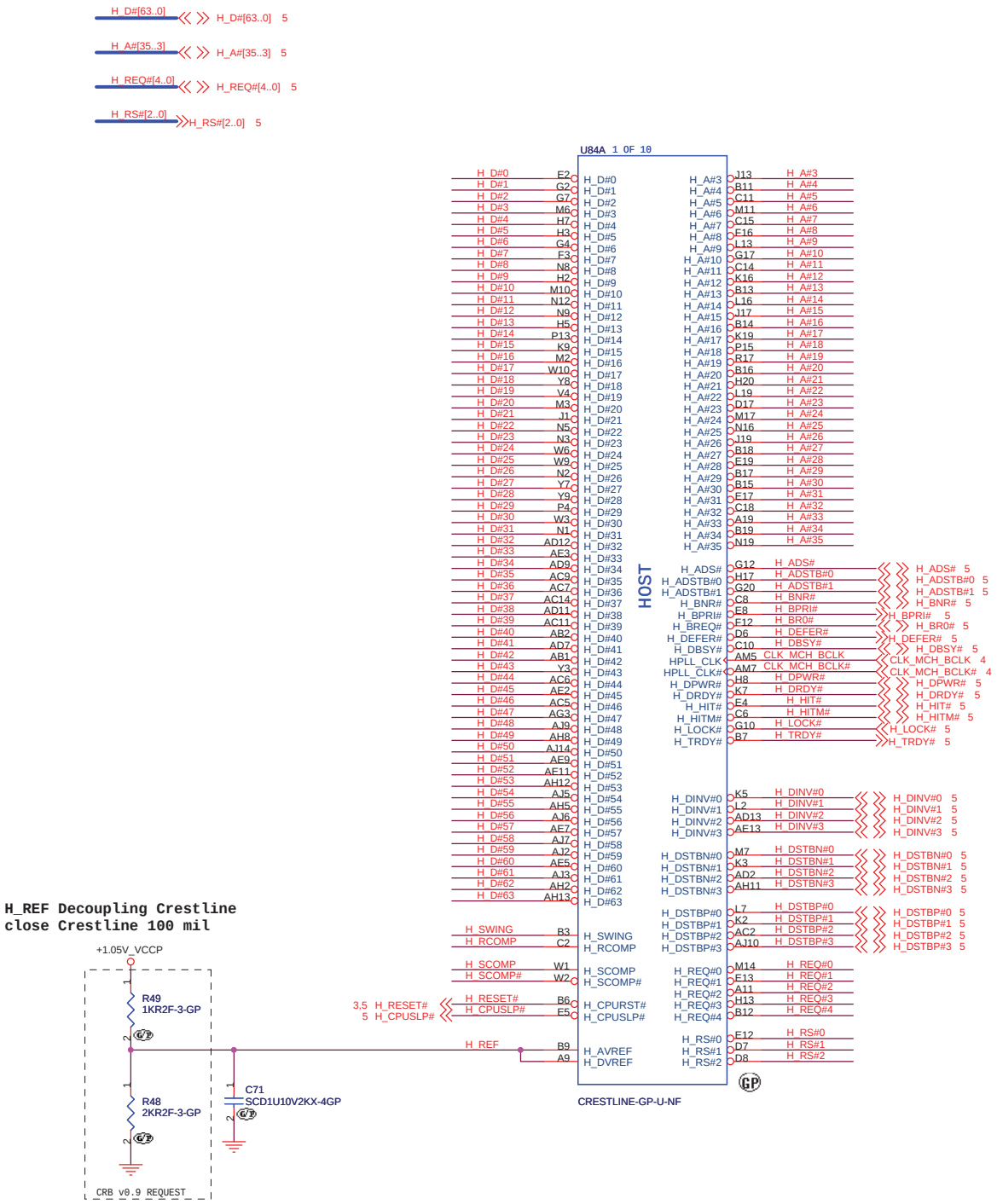

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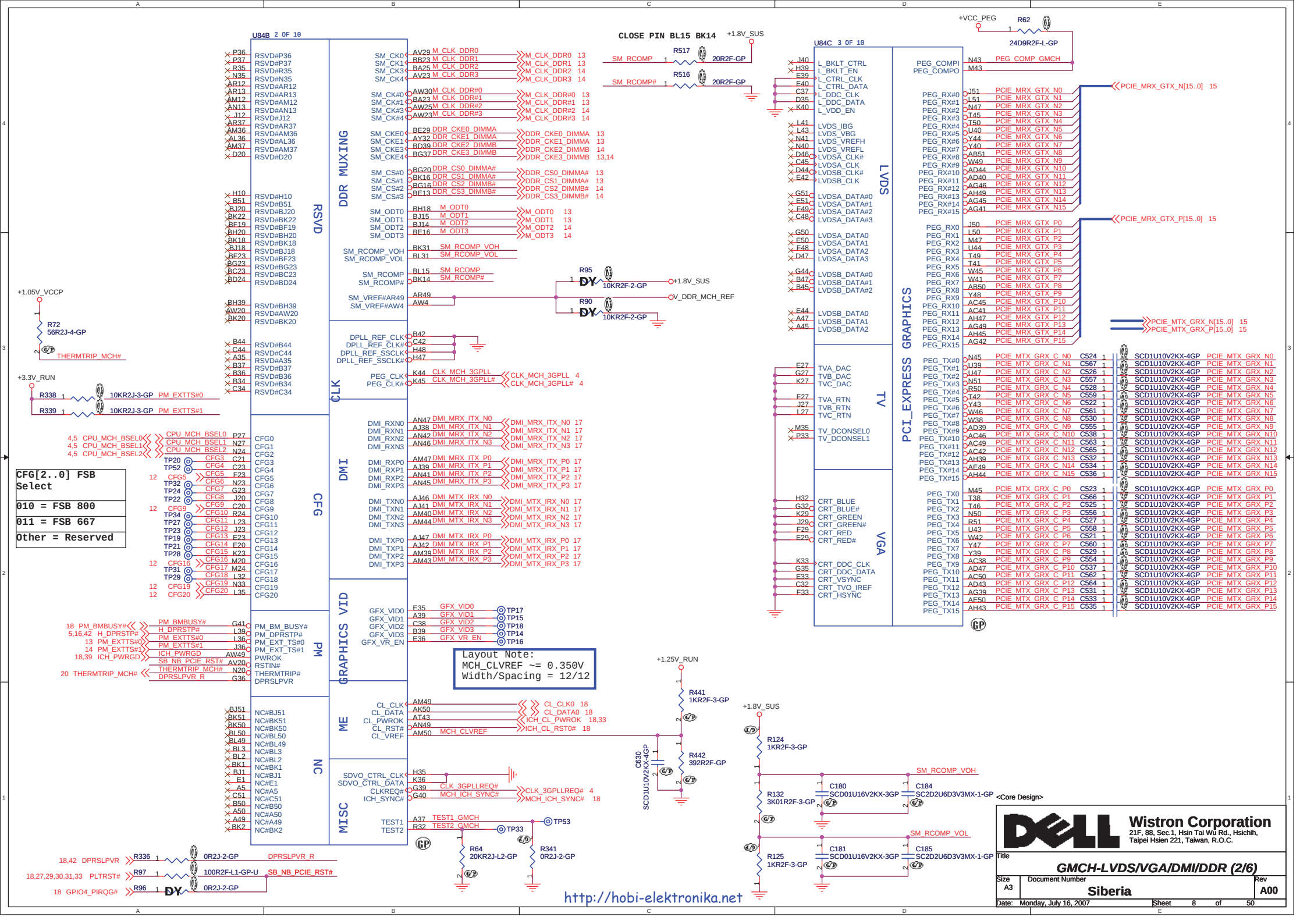
Title: GMCH-FSB LIBC (1/6)

Size: A3 | Document Number: Siberia | Rev: A00

Date: Monday, July 16, 2007 | Sheet 7 of 50


U84B 2 OF 10
RSVD
DDR MUXING
CLK
DMI
CFG
GRAPHICS VID
PM
ME
NC
MISC
CLOSE PIN BL15 BK14
+1.8V_SUS
R517 20R2F-GP
R516 20R2F-GP
SM_RCOMP
SM_RCOMP#
R95 10KR2F-2-GP
R90 10KR2F-2-GP
V_DDR_MCH_REF
+1.05V_VCCP
R72 56R2J-4-GP
THERMTRIP_MCH#
+3.3V_RUN
R338 10KR2J-3-GP PM_EXTTS#0
R339 10KR2J-3-GP PM_EXTTS#1
CFG[2..0] FSB Select
010 = FSB 800
011 = FSB 667
Other = Reserved
Layout Note:
MCH_CLVREF ~= 0.350V
Width/Spacing = 12/12
+1.25V_RUN
R441 1KR2F-3-GP
R442 392R2F-GP
C630 SCD1U10V2KX-4GP
R64 20KR2J-L2-GP
R341 0R2J-2-GP
R336 0R2J-2-GP DPRSLPVR_R
R97 100R2F-L1-GP-U SB_NB_PCIE_RST#
R96 0R2J-2-GP
U84C 3 OF 10
LVDS
TV
VGA
PCI_EXPRESS GRAPHICS
+VCC_PEG
R62 24D9R2F-L-GP
PEG_COMP_GMCH
PCIE_MRX_GTX_N[15..0] 15
PCIE_MRX_GTX_P[15..0] 15
PCIE_MTX_GRX_N[15..0] 15
PCIE_MTX_GRX_P[15..0] 15
SCD1U10V2KX-4GP
+1.8V_SUS
R124 1KR2F-3-GP
R132 3K01R2F-3-GP
C180 SCD01U16V2KX-3GP
C184 SC2D2U6D3V3MX-1-GP
SM_RCOMP_VOH
SM_RCOMP_VOL
R125 1KR2F-3-GP
C181 SCD01U16V2KX-3GP
C185 SC2D2U6D3V3MX-1-GP
<Core Design>
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Title
GMCH-LVDS/VGA/DMI/DDR (2/6)
Size A3
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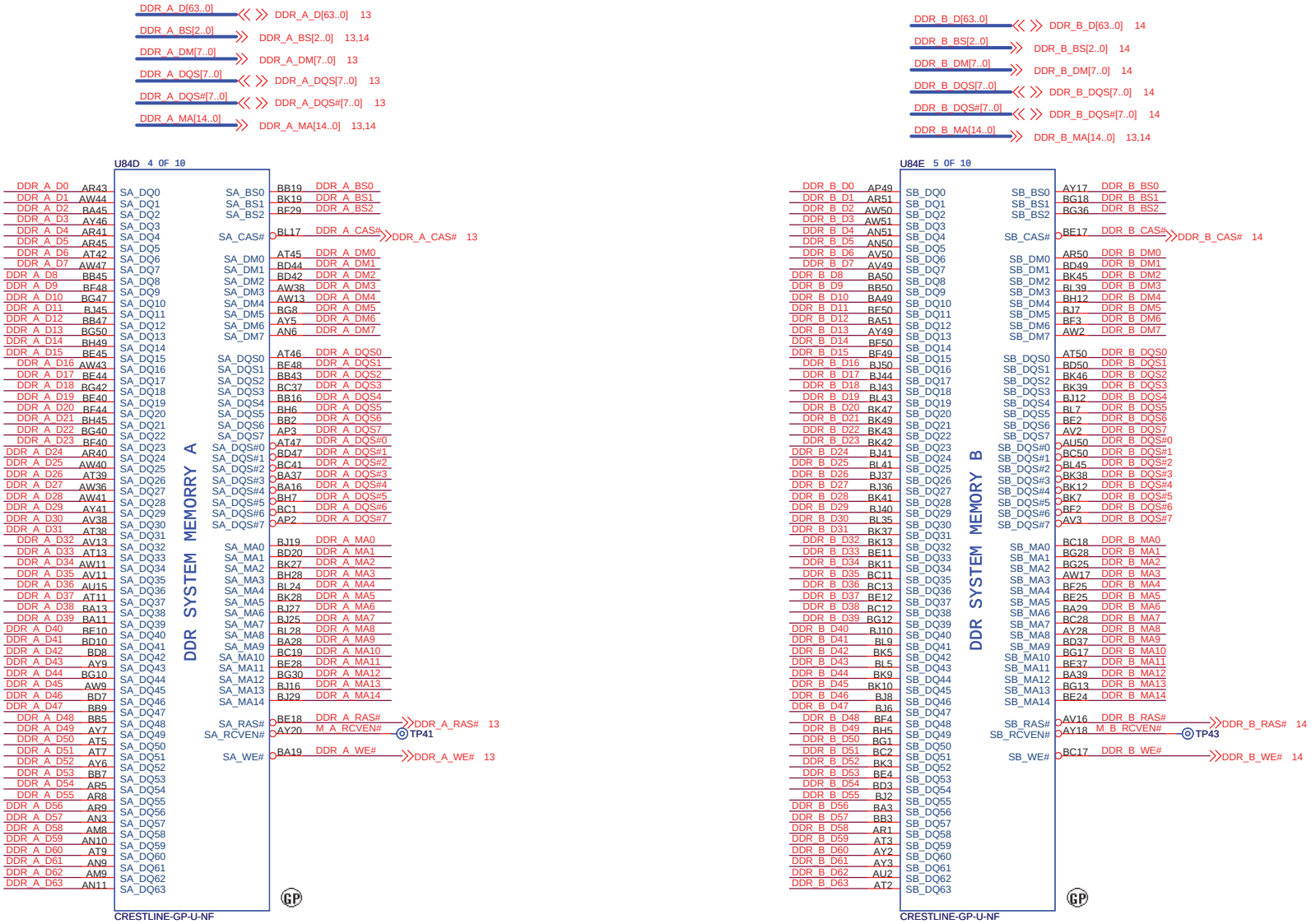

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Title: ***GMCH-DDR (3/6)***

Size: A3 | Document Number: **Siberia** | Rev: **A00**

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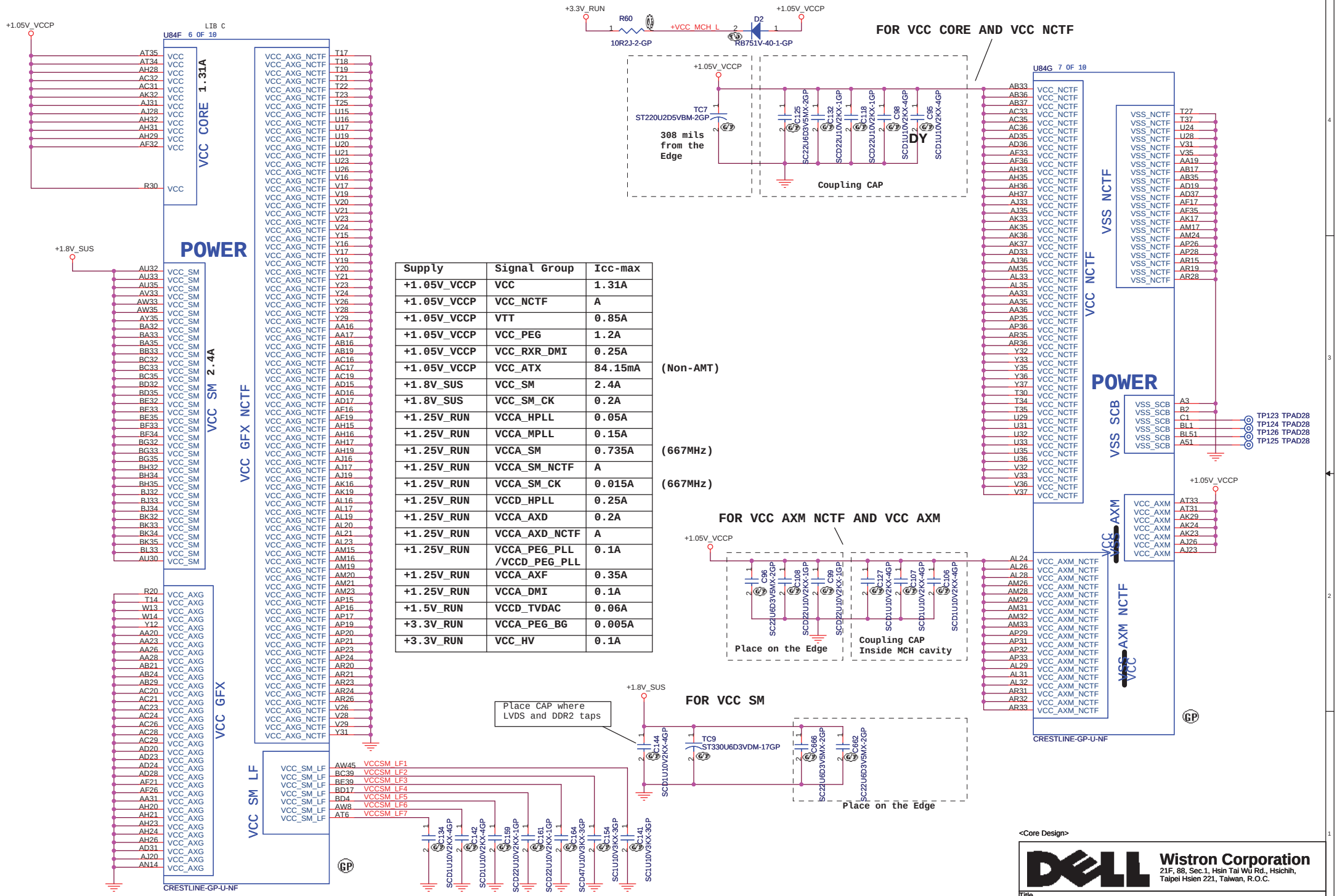

Supply	Signal Group	Icc-max	
+1.05V_VCCP	VCC	1.31A	
+1.05V_VCCP	VCC_NCTF	A	
+1.05V_VCCP	VTT	0.85A	
+1.05V_VCCP	VCC_PEG	1.2A	
+1.05V_VCCP	VCC_RXR_DMI	0.25A	
+1.05V_VCCP	VCC_ATX	84.15mA	(Non-AMT)
+1.8V_SUS	VCC_SM	2.4A	
+1.8V_SUS	VCC_SM_CK	0.2A	
+1.25V_RUN	VCCA_HPLL	0.05A	
+1.25V_RUN	VCCA_MPLL	0.15A	
+1.25V_RUN	VCCA_SM	0.735A	(667MHz)
+1.25V_RUN	VCCA_SM_NCTF	A	
+1.25V_RUN	VCCA_SM_CK	0.015A	(667MHz)
+1.25V_RUN	VCCD_HPLL	0.25A	
+1.25V_RUN	VCCA_AXD	0.2A	
+1.25V_RUN	VCCA_AXD_NCTF	A	
+1.25V_RUN	VCCA_PEG_PLL /VCCD_PEG_PLL	0.1A	
+1.25V_RUN	VCCA_AXF	0.35A	
+1.25V_RUN	VCCA_DMI	0.1A	
+1.5V_RUN	VCCD_TVDAC	0.06A	
+3.3V_RUN	VCCA_PEG_BG	0.005A	
+3.3V_RUN	VCC_HV	0.1A	

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Title: GMCH-POWER (4/6)

Size: A3 | Document Number: Siberia | Rev: A00

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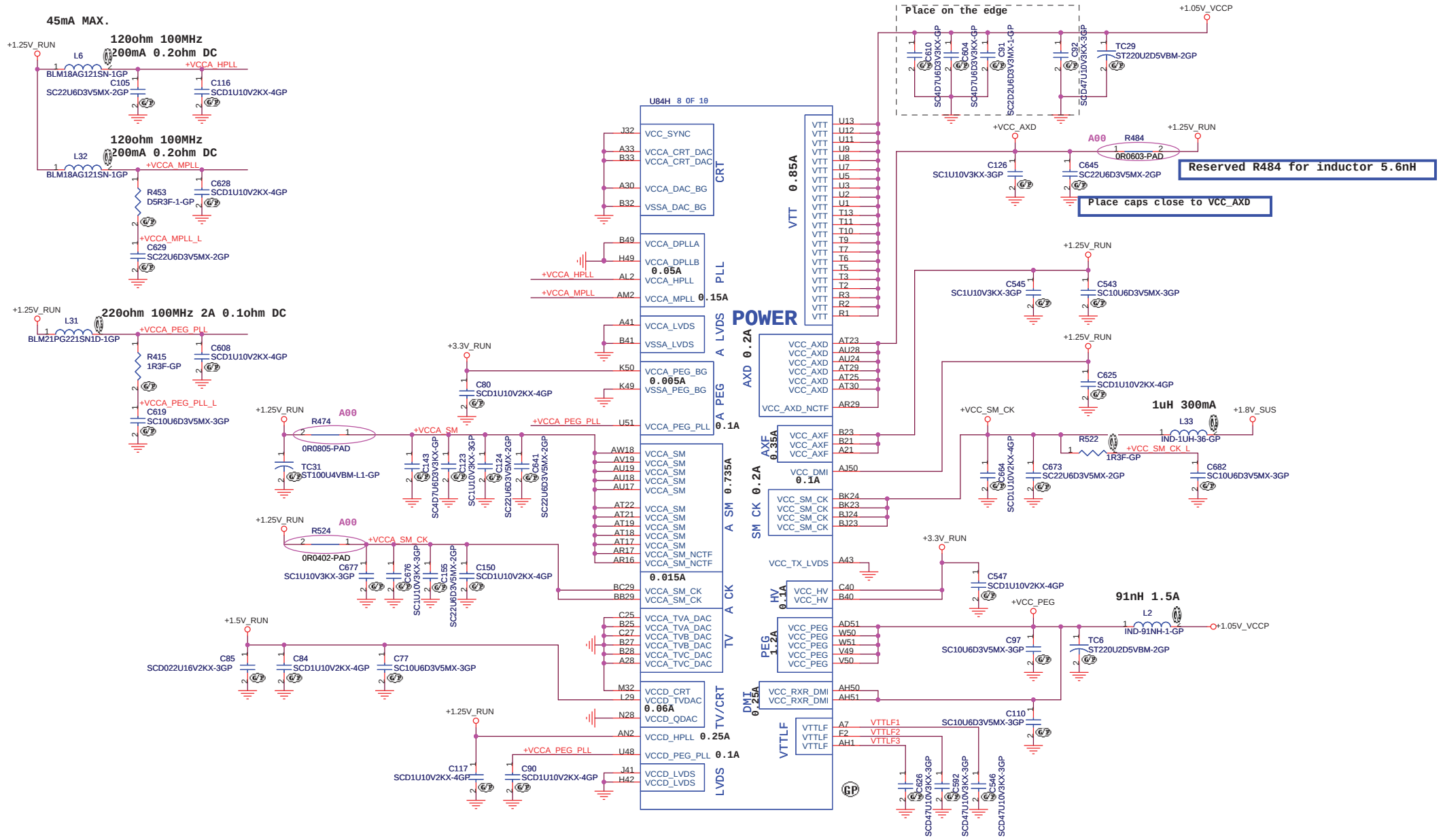

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Title: GMCH-POWER/FILTERR (5/6)

Size	Document Number	Rev
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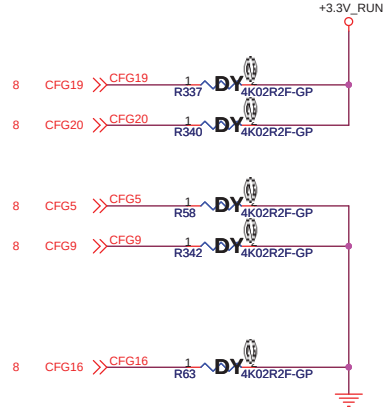
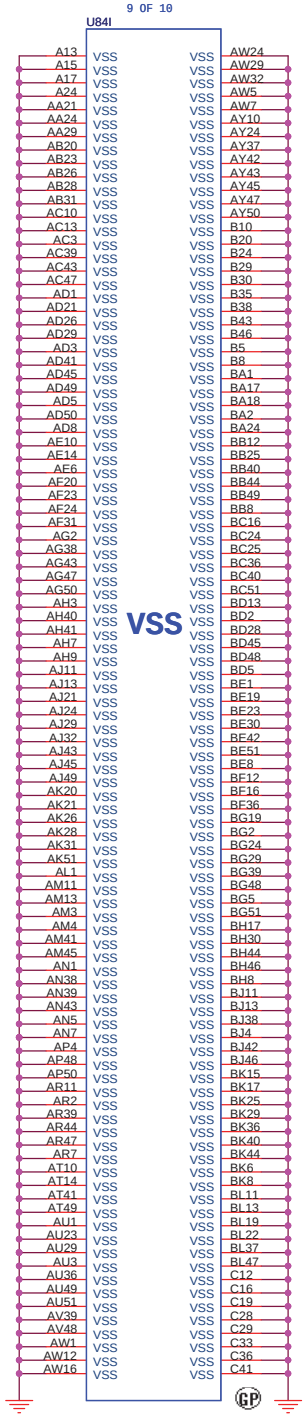
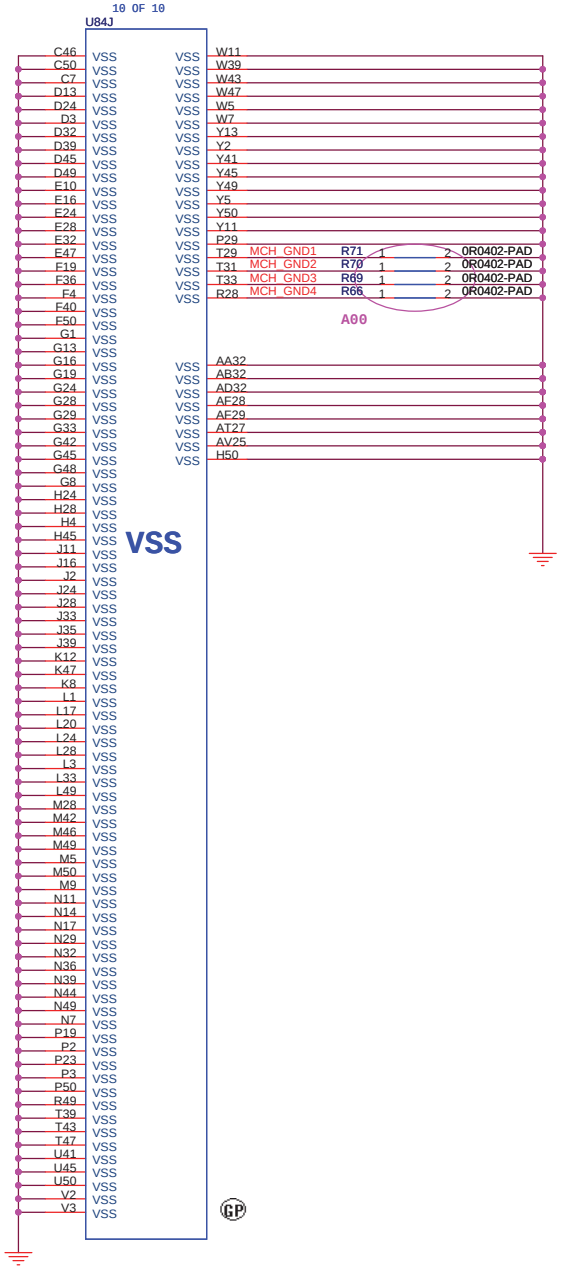
Layout Note:
Location of all MCH CFG strap resistors need to be close to trace to minimize stub



CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	★ DMI X 4
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	★ Normal Mode(Lanes number in order)
CFG 16 FSB Dynamic ODT	Disabled	★ Enabled
CFG 18 VCC select	★ 1.05V	1.5V
CFG 19 DMI Lane Reserved	★ Normal Operation	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	★ Only PCIE or SDVO is operation	PCIE and SDVO are operation simultaneous

CFG 12 CFG 13	XOR/ALL-Z
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation ★





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Title: ***GMCH-GND (6/6)***

Size: A3 | Document Number: **Siberia** | Rev: **A00**

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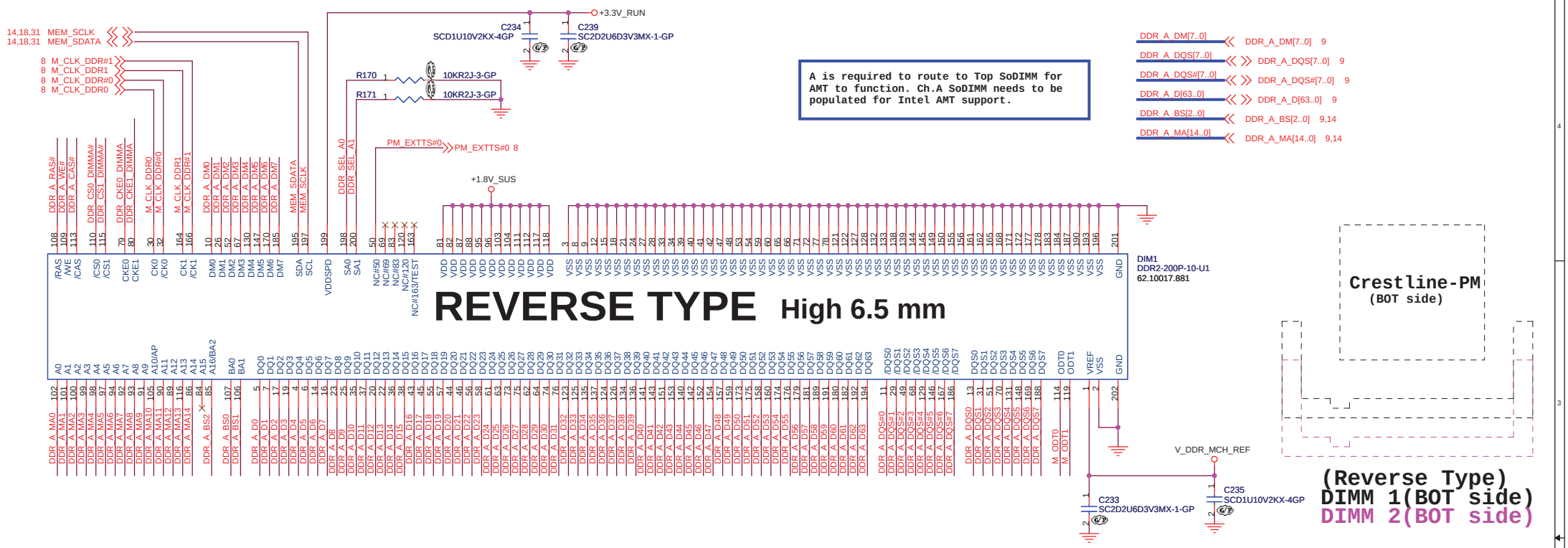
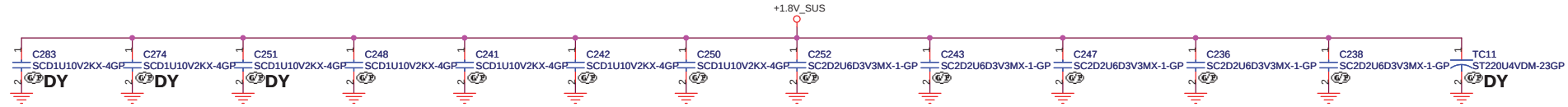
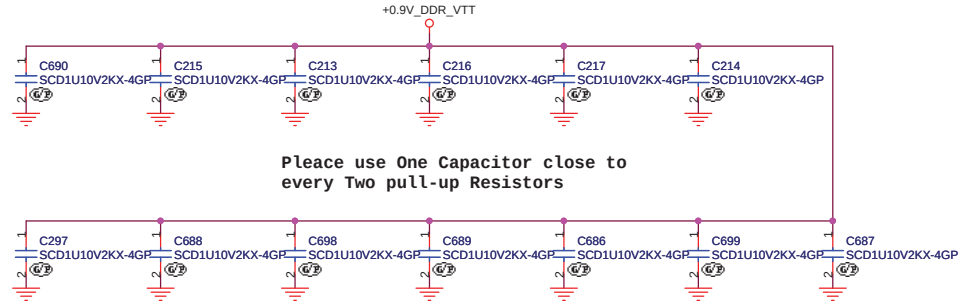
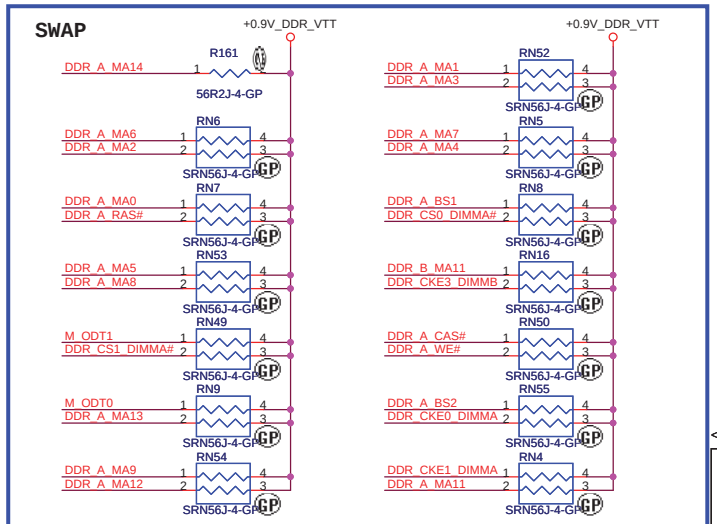




Pleace close to the DIMM Slot



Pleace use One Capacitor close to every Two pull-up Resistors



M_CKE[1:0] and M_CS[1:0]# pull-up Resistors close DIMM Slot 1300 mil (MAX)

Others pull-up Resistors close DIMM Slot 750 mil (MAX)

DDR_B_MA11 — DDR_B_MA11 9,14; DDR_CKE3_DIMMB — DDR_CKE3_DIMMB 8,14

DDR_CS0_DIMMA# — DDR_CS0_DIMMA# 8
DDR_CS1_DIMMA# — DDR_CS1_DIMMA# 8
DDR_CKE0_DIMMA — DDR_CKE0_DIMMA 8
DDR_CKE1_DIMMA — DDR_CKE1_DIMMA 8
DDR_A_RAS# — DDR_A_RAS# 9
DDR_A_CAS# — DDR_A_CAS# 9
DDR_A_WE# — DDR_A_WE# 9
M_ODT0 — M_ODT0 8
M_ODT1 — M_ODT1 8

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR2-SODIMM1

Size: A3 | Document Number: Siberia | Rev: A00

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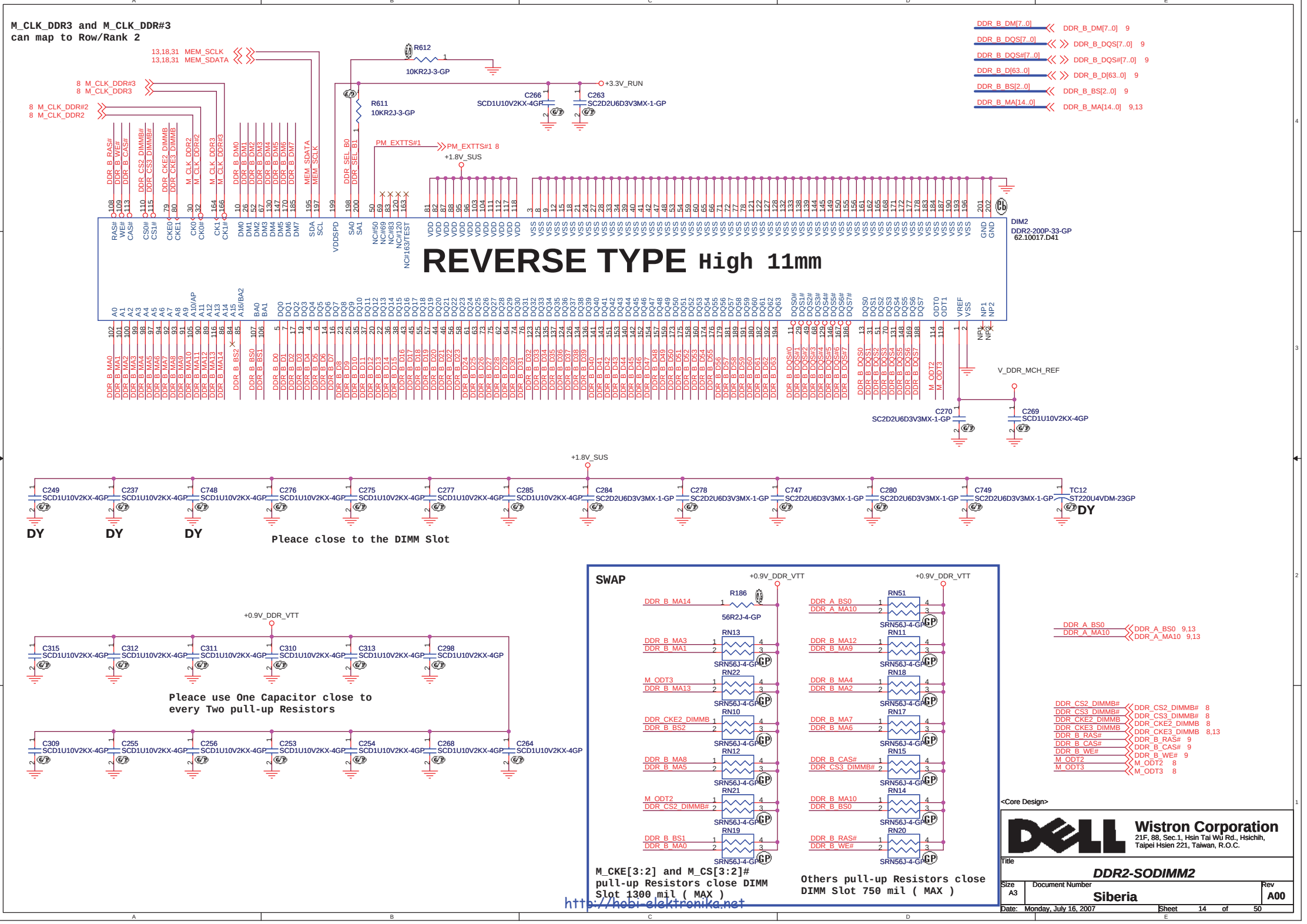
M_CLK_DDR3 and M_CLK_DDR#3
can map to Row/Rank 2
13,18,31 MEM_SCLK
13,18,31 MEM_SDATA
8 M_CLK_DDR#3
8 M_CLK_DDR3
8 M_CLK_DDR#2
8 M_CLK_DDR2
R612
10KR2J-3-GP
R611
10KR2J-3-GP
+3.3V_RUN
C266
SCD1U10V2KX-4GP
C263
SC2D2U6D3V3MX-1-GP
PM_EXTTS#1
PM_EXTTS#1 8
+1.8V_SUS
DDR_B_DM[7..0]
DDR_B_DQS[7..0]
DDR_B_DQS#[7..0]
DDR_B_D[63..0]
DDR_B_BS[2..0]
DDR_B_MA[14..0]
DIM2
DDR2-200P-33-GP
62.10017.D41
REVERSE TYPE High 11mm
V_DDR_MCH_REF
C270
SC2D2U6D3V3MX-1-GP
C269
SCD1U10V2KX-4GP
+1.8V_SUS
C249
SCD1U10V2KX-4GP
C237
SCD1U10V2KX-4GP
C748
SCD1U10V2KX-4GP
C276
SCD1U10V2KX-4GP
C275
SCD1U10V2KX-4GP
C277
SCD1U10V2KX-4GP
C285
SCD1U10V2KX-4GP
C284
SC2D2U6D3V3MX-1-GP
C278
SC2D2U6D3V3MX-1-GP
C747
SC2D2U6D3V3MX-1-GP
C280
SC2D2U6D3V3MX-1-GP
C749
SC2D2U6D3V3MX-1-GP
TC12
ST220U4VDM-23GP
DY
DY
DY
DY
Please close to the DIMM Slot
+0.9V_DDR_VTT
C315
SCD1U10V2KX-4GP
C312
SCD1U10V2KX-4GP
C311
SCD1U10V2KX-4GP
C310
SCD1U10V2KX-4GP
C313
SCD1U10V2KX-4GP
C298
SCD1U10V2KX-4GP
Please use One Capacitor close to
every Two pull-up Resistors
C309
SCD1U10V2KX-4GP
C255
SCD1U10V2KX-4GP
C256
SCD1U10V2KX-4GP
C253
SCD1U10V2KX-4GP
C254
SCD1U10V2KX-4GP
C268
SCD1U10V2KX-4GP
C264
SCD1U10V2KX-4GP
SWAP
+0.9V_DDR_VTT
+0.9V_DDR_VTT
R186
56R2J-4-GP
RN51
SRN56J-4-GP
RN13
RN11
RN22
RN18
RN10
RN17
RN12
RN15
RN21
RN14
RN19
RN20
DDR_B_MA14
DDR_B_MA3
DDR_B_MA1
M_ODT3
DDR_B_MA13
DDR_CKE2_DIMMB
DDR_B_BS2
DDR_B_MA8
DDR_B_MA5
M_ODT2
DDR_CS2_DIMMB#
DDR_B_BS1
DDR_B_MA0
DDR_A_BS0
DDR_A_MA10
DDR_B_MA12
DDR_B_MA9
DDR_B_MA4
DDR_B_MA2
DDR_B_MA7
DDR_B_MA6
DDR_B_CAS#
DDR_CS3_DIMMB#
DDR_B_MA10
DDR_B_BS0
DDR_B_RAS#
DDR_B_WE#
M_CKE[3:2] and M_CS[3:2]#
pull-up Resistors close DIMM
Slot 1300 mil (MAX)
Others pull-up Resistors close
DIMM Slot 750 mil (MAX)
DDR_A_BS0 9,13
DDR_A_MA10 9,13
DDR_CS2_DIMMB# 8
DDR_CS3_DIMMB# 8
DDR_CKE2_DIMMB 8
DDR_CKE3_DIMMB 8,13
DDR_B_RAS# 9
DDR_B_CAS# 9
DDR_B_WE# 9
M_ODT2 8
M_ODT3 8
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR2-SODIMM2
Size A3
Document Number
Siberia
Rev A00
Date: Monday, July 16, 2007
Sheet 14 of 50
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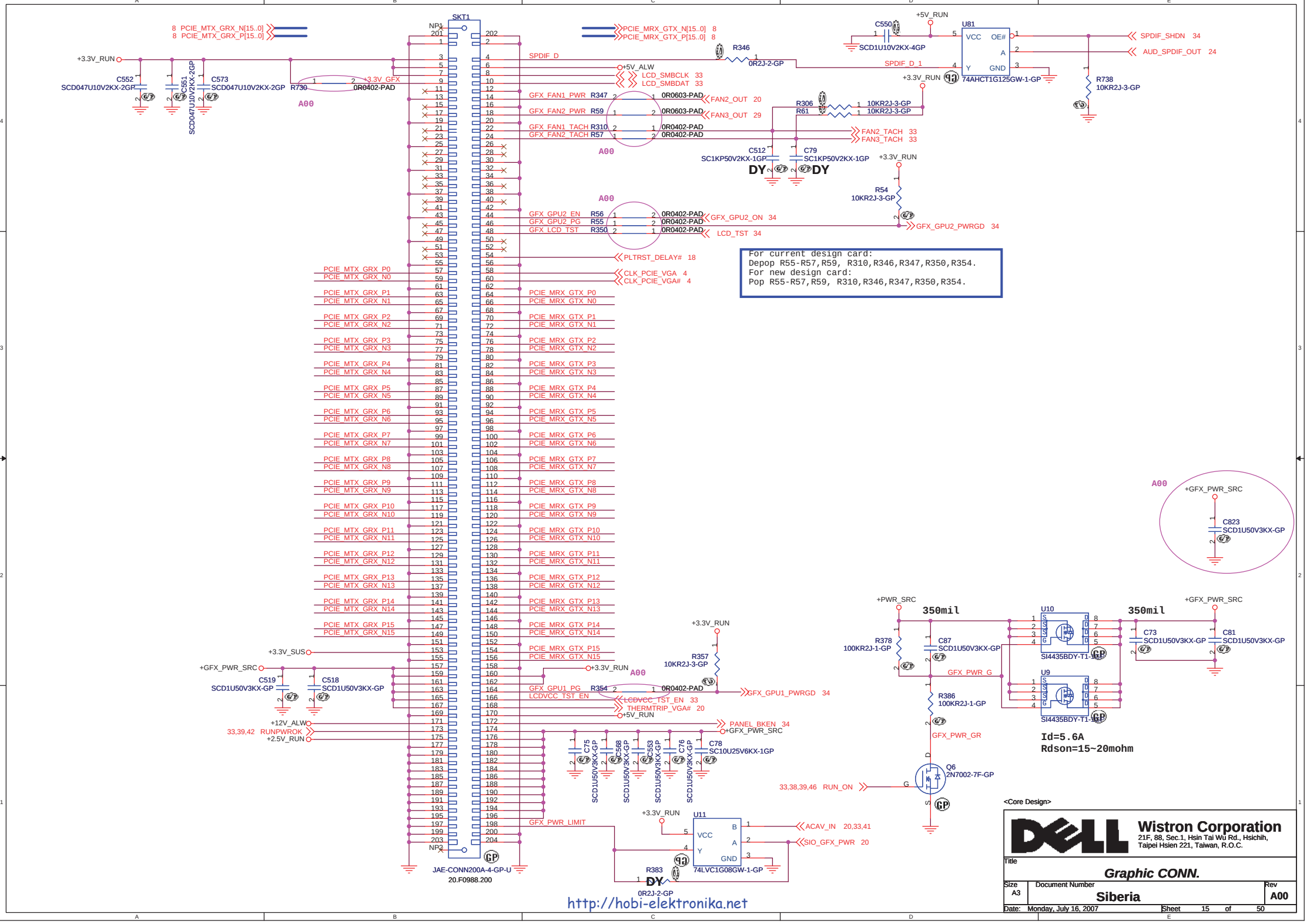
SKT1
JAE-CONN200A-4-GP-U
20.F0988.200
8 PCIE_MTX_GRX_N[15..0]
8 PCIE_MTX_GRX_P[15..0]
PCIE_MRX_GTX_N[15..0] 8
PCIE_MRX_GTX_P[15..0] 8
+3.3V_RUN
C552 SCD047U10V2KX-2GP
C551 SCD047U10V2KX-2GP
C573 SCD047U10V2KX-2GP
R730 0R0402-PAD
+3.3V_GFX
A00
SPDIF_D
R346 0R2J-2-GP
+5V_ALW
LCD_SMBCLK 33
LCD_SMBDAT 33
GFX_FAN1_PWR R347 0R0603-PAD
GFX_FAN2_PWR R59 0R0603-PAD
GFX_FAN1_TACH R310 0R0402-PAD
GFX_FAN2_TACH R57 0R0402-PAD
FAN2_OUT 20
FAN3_OUT 29
FAN2_TACH 33
FAN3_TACH 33
C550 SCD1U10V2KX-4GP
+5V_RUN
U81 74AHCT1G125GW-1-GP
VCC OE# A Y GND
SPDIF_D_1
SPDIF_SHDN 34
AUD_SPDIF_OUT 24
R738 10KR2J-3-GP
R306 10KR2J-3-GP
R61 10KR2J-3-GP
C512 SC1KP50V2KX-1GP
C79 SC1KP50V2KX-1GP
DY
R54 10KR2J-3-GP
GFX_GPU2_EN R56 0R0402-PAD
GFX_GPU2_PG R55 0R0402-PAD
GFX_LCD_TST R350 0R0402-PAD
GFX_GPU2_ON 34
LCD_TST 34
GFX_GPU2_PWRGD 34
PLTRST_DELAY# 18
CLK_PCIE_VGA 4
CLK_PCIE_VGA# 4
PCIE_MTX_GRX_P0
PCIE_MTX_GRX_N0
PCIE_MRX_GTX_P0
PCIE_MRX_GTX_N0
+3.3V_SUS
+GFX_PWR_SRC
C519 SCD1U50V3KX-GP
C518 SCD1U50V3KX-GP
R357 10KR2J-3-GP
GFX_GPU1_PG R354 0R0402-PAD
GFX_GPU1_PWRGD 34
LCDVCC_TST_EN
LCDVCC_TST_EN 33
THERMTRIP_VGA# 20
+5V_RUN
+12V_ALW
33,39,42 RUNPWROK
+2.5V_RUN
PANEL_BKEN 34
C75 SCD1U50V3KX-GP
C568 SCD1U50V3KX-GP
C553 SCD1U50V3KX-GP
C76 SCD1U50V3KX-GP
C78 SC10U25V6KX-1GP
GFX_PWR_LIMIT
U11 74LVC1G08GW-1-GP
VCC B A Y GND
ACAV_IN 20,33,41
SIO_GFX_PWR 20
R383 0R2J-2-GP
http://hobi-elektronika.net
For current design card:
Depop R55-R57,R59, R310,R346,R347,R350,R354.
For new design card:
Pop R55-R57,R59, R310,R346,R347,R350,R354.
+GFX_PWR_SRC
C823 SCD1U50V3KX-GP
+PWR_SRC
350mil
R378 100KR2J-1-GP
C87 SCD1U50V3KX-GP
GFX_PWR_G
R386 100KR2J-1-GP
GFX_PWR_GR
Q6 2N7002-7F-GP
33,38,39,46 RUN_ON
U10 SI4435BDY-T1-GP
U9 SI4435BDY-T1-GP
Id=5.6A
Rdson=15~20mohm
C73 SCD1U50V3KX-GP
C81 SCD1U50V3KX-GP
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Graphic CONN.
Size A3
Document Number
Siberia
Rev A00
Date: Monday, July 16, 2007
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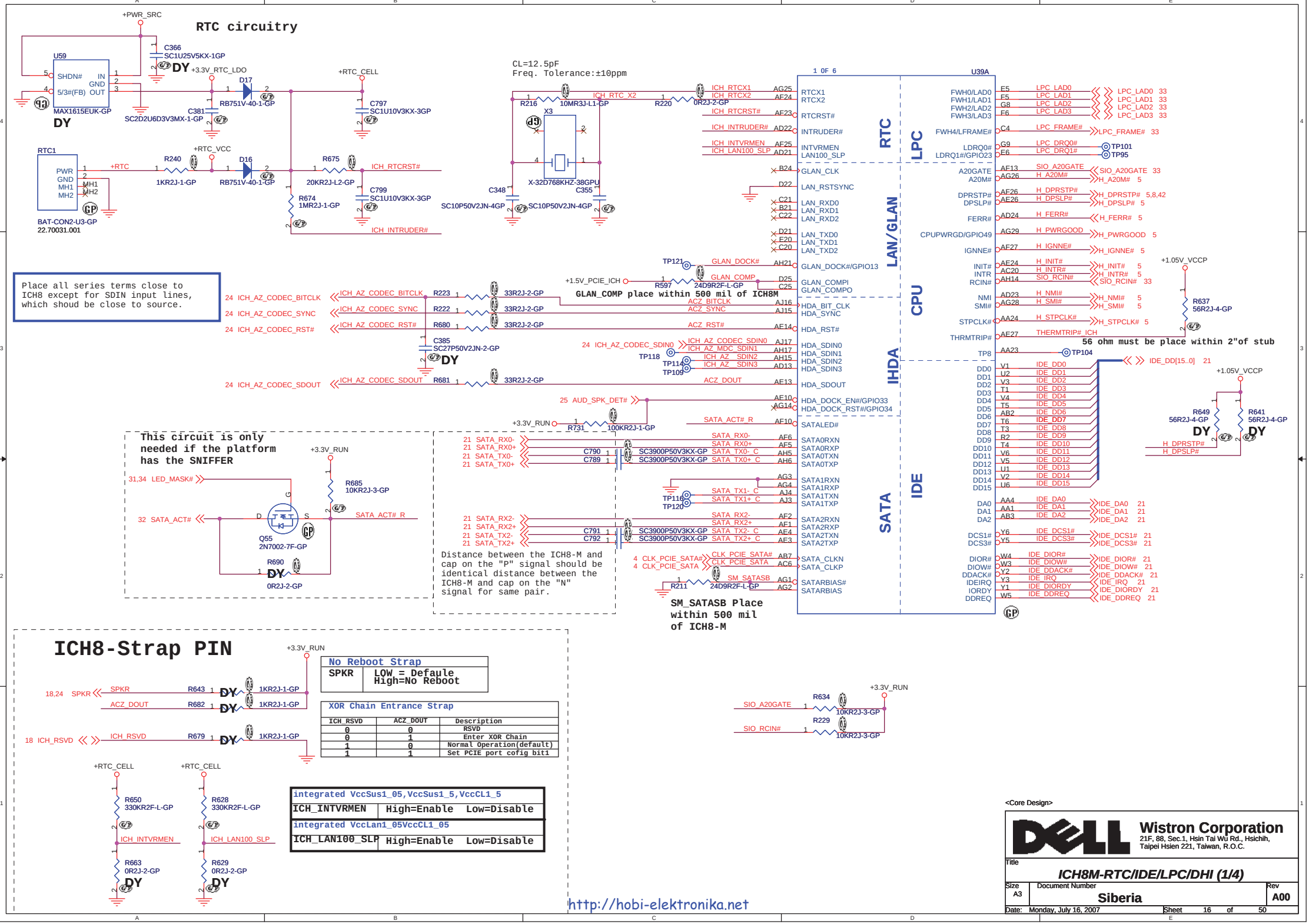
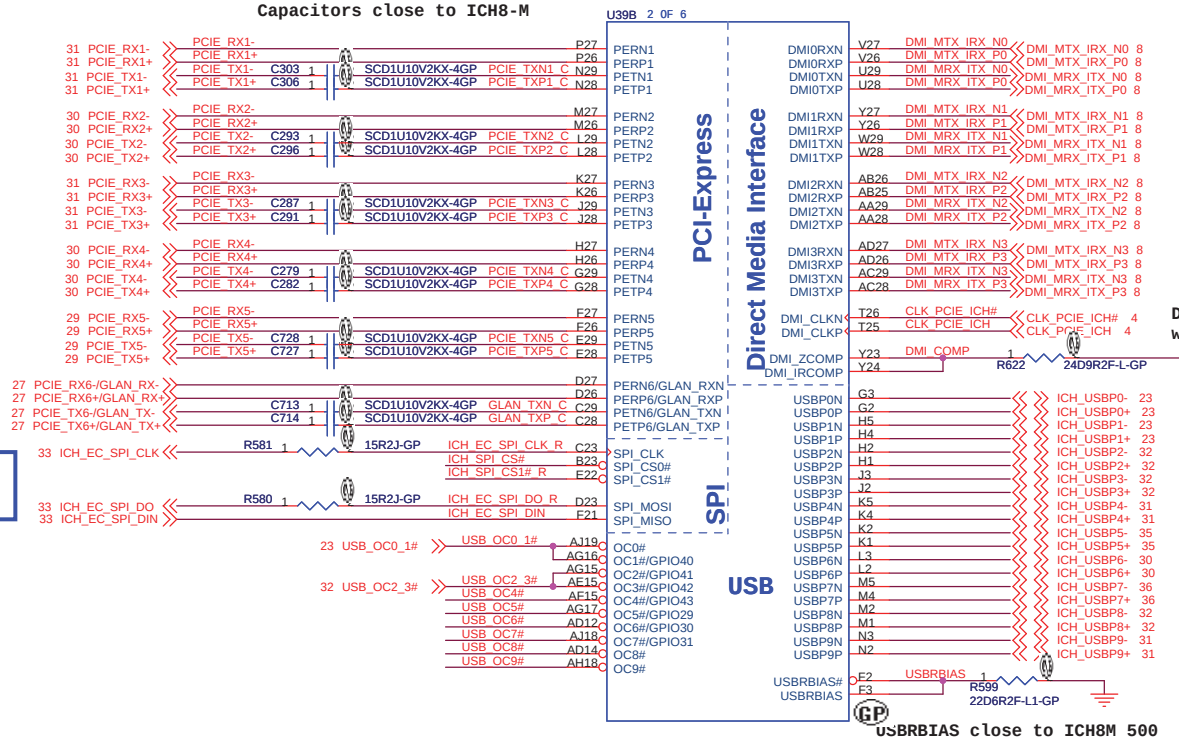

RTC circuitry
+PWR_SRC
U59
SHDN#
5/3#(FB)
IN
GND
OUT
MAX1615EUK-GP
DY
C366
SC1U25V5KX-1GP
+3.3V_RTC_LDO
C381
SC2D2U6D3V3MX-1-GP
D17
RB751V-40-1-GP
+RTC_CELL
C797
SC1U10V3KX-3GP
RTC1
PWR
GND
MH1
MH2
BAT-CON2-U3-GP
22.70031.001
+RTC
R240
1KR2J-1-GP
+RTC_VCC
D16
RB751V-40-1-GP
R675
20KR2J-L2-GP
ICH_RTCRST#
C799
SC1U10V3KX-3GP
R674
1MR2J-1-GP
ICH_INTRUDER#
CL=12.5pF
Freq. Tolerance:±10ppm
R216
10MR3J-L1-GP
ICH_RTC_X2
R220
0R2J-2-GP
X3
X-32D768KHZ-38GPU
C348
SC10P50V2JN-4GP
C355
SC10P50V2JN-4GP
1 0F 6
U39A
ICH_RTCX1
ICH_RTCX2
RTCX1
RTCX2
ICH_RTCRST#
RTCRST#
ICH_INTRUDER#
INTRUDER#
ICH_INTVRMEN
ICH_LAN100_SLP
INTVRMEN
LAN100_SLP
RTC
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#
GLAN_DOCK#/GPIO13
GLAN_COMP
GLAN_COMPI
GLAN_COMPO
LAN/GLAN
+1.5V_PCIE_ICH
R597
24D9R2F-L-GP
GLAN_COMP place within 500 mil of ICH8M
Place all series terms close to ICH8 except for SDIN input lines, which shoud be close to source.
24 ICH_AZ_CODEC_BITCLK
24 ICH_AZ_CODEC_SYNC
24 ICH_AZ_CODEC_RST#
ICH_AZ_CODEC_BITCLK
ICH_AZ_CODEC_SYNC
ICH_AZ_CODEC_RST#
R223
R222
R680
33R2J-2-GP
C385
SC27P50V2JN-2-GP
DY
ACZ_BITCLK
ACZ_SYNC
ACZ_RST#
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
24 ICH_AZ_CODEC_SDIN0
ICH_AZ_CODEC_SDIN0
ICH_AZ_MDC_SDIN1
ICH_AZ_SDIN2
ICH_AZ_SDIN3
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
24 ICH_AZ_CODEC_SDOUT
ICH_AZ_CODEC_SDOUT
R681
ACZ_DOUT
HDA_SDOUT
IHDA
25 AUD_SPK_DET#
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
+3.3V_RUN
R731
100KR2J-1-GP
SATA_ACT# R
SATALED#
This circuit is only needed if the platform has the SNIFFER
31,34 LED_MASK#
32 SATA_ACT#
R685
10KR2J-3-GP
Q55
2N7002-7F-GP
R690
0R2J-2-GP
21 SATA_RX0-
21 SATA_RX0+
21 SATA_TX0-
21 SATA_TX0+
C790
C789
SC3900P50V3KX-GP
SATA_RX0-
SATA_RX0+
SATA_TX0- C
SATA_TX0+ C
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA_TX1- C
SATA_TX1+ C
TP118
TP120
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
21 SATA_RX2-
21 SATA_RX2+
21 SATA_TX2-
21 SATA_TX2+
C791
C792
SATA_RX2-
SATA_RX2+
SATA_TX2- C
SATA_TX2+ C
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
Distance between the ICH8-M and cap on the "P" signal should be identical distance between the ICH8-M and cap on the "N" signal for same pair.
4 CLK_PCIE_SATA#
4 CLK_PCIE_SATA
CLK_PCIE_SATA#
CLK_PCIE_SATA
SATA_CLKN
SATA_CLKP
R211
24D9R2F-L-GP
SM_SATASB
SATARBIAS#
SATARBIAS
SM_SATASB Place within 500 mil of ICH8-M
SATA
LPC
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
LPC_LAD0
LPC_LAD1
LPC_LAD2
LPC_LAD3
LPC_FRAME#
LPC_DRQ0#
LPC_DRQ1#
TP101
TP95
A20GATE
A20M#
SIO_A20GATE
H_A20M#
DPRSTP#
DPSLP#
H_DPRSTP#
H_DPSLP#
FERR#
H_FERR#
CPUPWRGD/GPIO49
H_PWRGOOD
IGNNE#
H_IGNNE#
INIT#
INTR
RCIN#
H_INIT#
H_INTR#
SIO_RCIN#
NMI
SMI#
H_NMI#
H_SMI#
STPCLK#
H_STPCLK#
THRMTRIP#
THERMTRIP# ICH
TP8
TP104
CPU
+1.05V_VCCP
R637
56R2J-4-GP
56 ohm must be place within 2"of stub
IDE_DD[15..0]
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
IDE_DD0
IDE_DD1
IDE_DD2
IDE_DD3
IDE_DD4
IDE_DD5
IDE_DD6
IDE_DD7
IDE_DD8
IDE_DD9
IDE_DD10
IDE_DD11
IDE_DD12
IDE_DD13
IDE_DD14
IDE_DD15
R649
56R2J-4-GP
R641
56R2J-4-GP
DA0
DA1
DA2
IDE_DA0
IDE_DA1
IDE_DA2
DCS1#
DCS3#
IDE_DCS1#
IDE_DCS3#
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
IDE_DIOR#
IDE_DIOW#
IDE_DDACK#
IDE_IRQ
IDE_IORDY
IDE_DDREQ
IDE
ICH8-Strap PIN
+3.3V_RUN
No Reboot Strap
SPKR
LOW = Defaule
High=No Reboot
18,24 SPKR
ACZ_DOUT
R643
R682
1KR2J-1-GP
18 ICH_RSVD
ICH_RSVD
R679
XOR Chain Entrance Strap
ICH_RSVD
ACZ_DOUT
Description
0 0 RSVD
0 1 Enter XOR Chain
1 0 Normal Operation(default)
1 1 Set PCIE port cofig bit1
+RTC_CELL
R650
330KR2F-L-GP
ICH_INTVRMEN
R663
0R2J-2-GP
R628
330KR2F-L-GP
ICH_LAN100_SLP
R629
0R2J-2-GP
integrated VccSus1_05,VccSus1_5,VccCL1_5
ICH_INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
ICH_LAN100_SLP High=Enable Low=Disable
SIO_A20GATE
SIO_RCIN#
R634
R229
10KR2J-3-GP
http://hobi-elektronika.net
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8M-RTC/IDE/LPC/DHI (1/4)
Size A3
Document Number
Siberia
Rev A00
Date: Monday, July 16, 2007
Sheet 16 of 50

PCIE Interface Routing

LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	MiniCard WPAN
LANE4	Express Card
LANE5	PPU Card
LANE6	Giba Bit LOM

PCIE TX dc blocking
Capacitors close to ICH8-M



DMI_COMP R622 place within 500 mil of ICH8M

USBRBIAS close to ICH8M 500 mils and Trace impedance should be 60 ohm +/- 15%

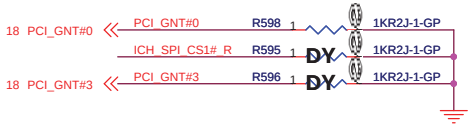
Layout Note:
Place R563, R580 and R581 within 500 mils from ICH.

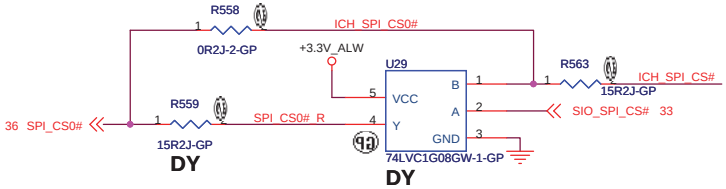
ICH

USB0	Ext Left Side
USB1	Ext Back
USB2	Ext Right Side (Top)
USB3	Ext Right Side (Bottom)
USB4	3rd mini card
USB5	Camera
USB6	Express Card
USB7	BT
USB8	Gaming LCD
USB9	WWAN

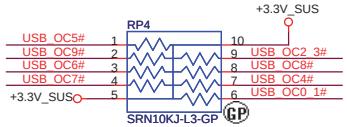
ICH8-Strap PIN

BOOT BIOS Strap		
PCI_GNT#0 (R617)	SPI_CS#1 (R623)	BOOT BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC
A16 swap override strap		
PCI_GNT#3 (R620)	low = A16 swap override enable high = default	





USB OC# PULL HIGH



http://hobi-elektronika.net

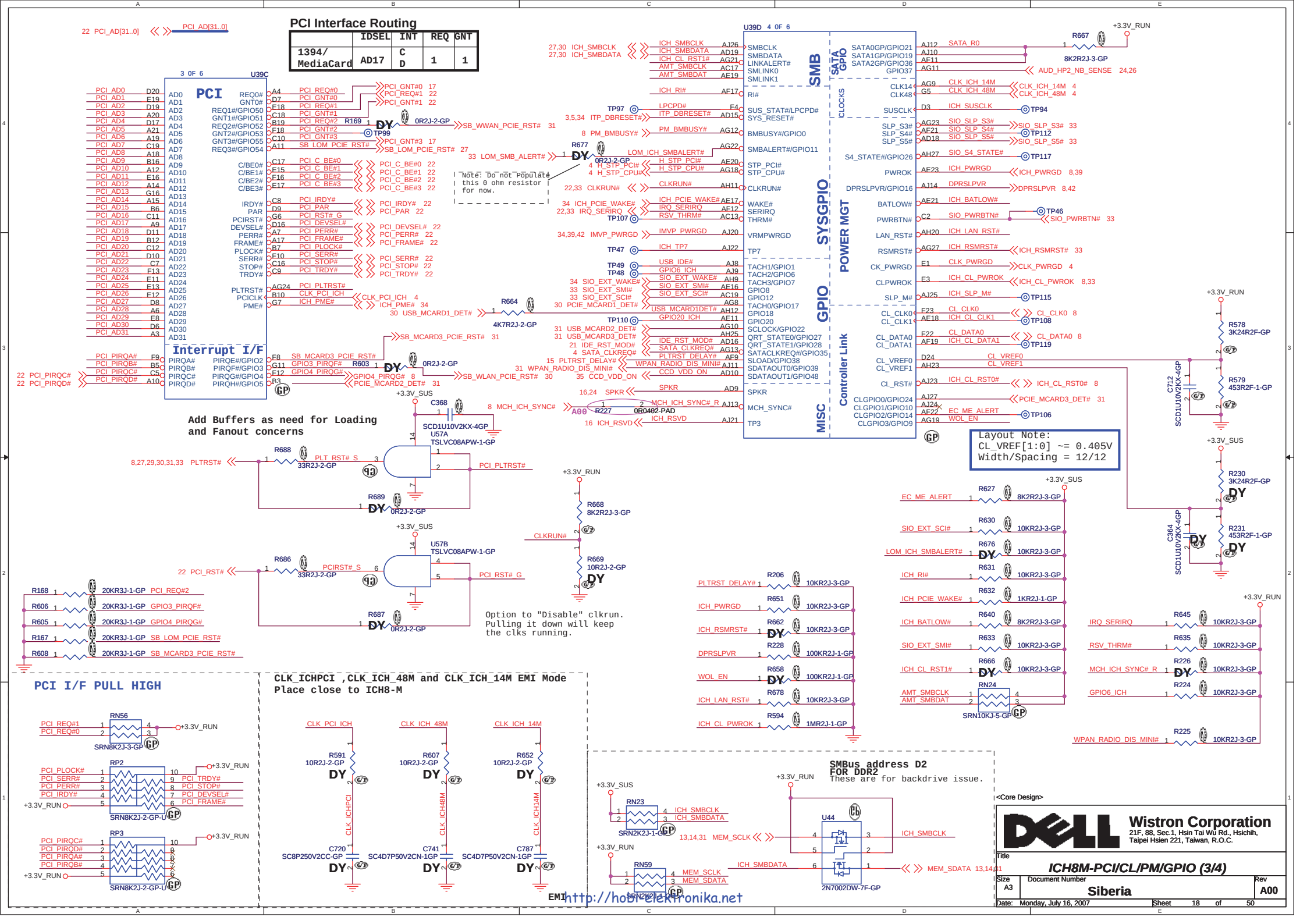
<Core Design>

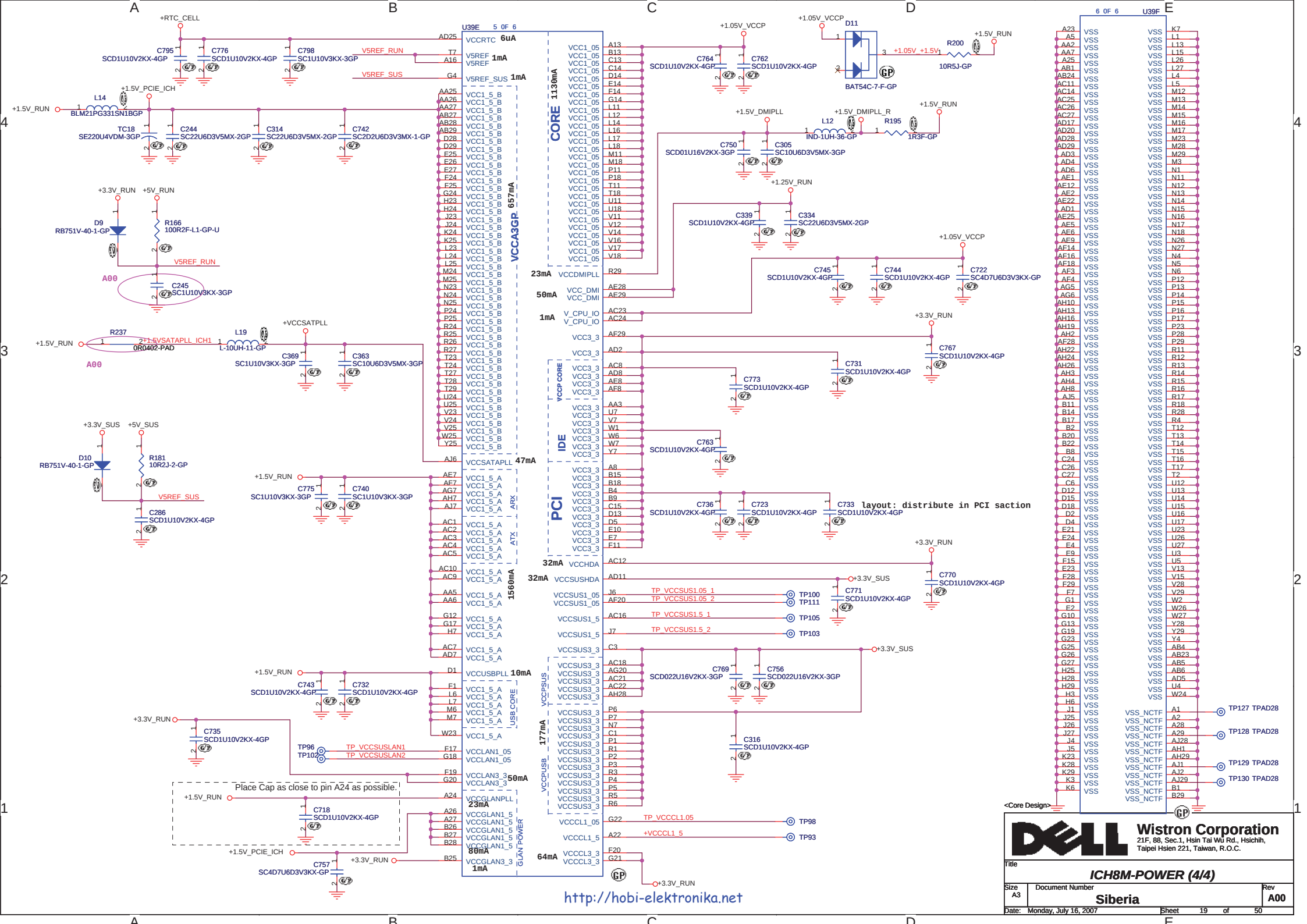
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH8M-PCIE/USB/SPI/DMI (2/4)

Size: A3 | Document Number: Siberia | Rev: A00

Date: Monday, July 16, 2007 | Sheet 17 of 50


PCI Interface Routing
IDSEL INT REQ GNT
1394/ MediaCard AD17 C D 1 1
PCI
Interrupt I/F
U39C
U39D 4 0F 6
SMB
SATA GPIO
CLOCKS
SYSGPIO
POWER MGT
GPIO
Controller Link
MISC
Add Buffers as need for Loading and Fanout concerns
Layout Note:
CL_VREF[1:0] ~= 0.405V
Width/Spacing = 12/12
Note: Do not populate this 0 ohm resistor for now.
Option to "Disable" clkrun. Pulling it down will keep the clks running.
PCI I/F PULL HIGH
CLK_ICHPCI ,CLK_ICH_48M and CLK_ICH_14M EMI Mode
Place close to ICH8-M
SMBus address D2
FOR DDR2
These are for backdrive issue.
EMI
http://hobi-elektronika.net
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH8M-PCI/CL/PM/GPIO (3/4)
Size A3
Document Number
Siberia
Rev A00
Date: Monday, July 16, 2007
Sheet 18 of 50


U39E 5 OF 6
VCCRTC 6uA
V5REF 1mA
V5REF_SUS 1mA
VCCA3GP 657mA
VCCSATAPLL 47mA
VCCUSBPLL 10mA
VCCLANPLL 23mA
VCCGLANPLL 80mA
VCCGLAN3_3 1mA
VCCDMIPLL 23mA
VCC_DMI 50mA
V_CPU_IO 1mA
VCCSUSHDA 32mA
VCCLAN3_3 50mA
VCCCL3_3 64mA
CORE 1130mA
PCI 1560mA
IDE
VCCP CORE
APX
ATX
USB_CORE
VCCPSUS 177mA
VCCPUSB
GLAN POWER
U39F 6 OF 6
VSS
VSS_NCTF
<Core Design>
Place Cap as close to pin A24 as possible.
layout: distribute in PCI saction
TP_VCCSUS1.05_1
TP_VCCSUS1.05_2
TP_VCCSUS1.5_1
TP_VCCSUS1.5_2
TP_VCCSUSLAN1
TP_VCCSUSLAN2
TP_VCCCL1.05
+VCCCL1_5
TP127 TPAD28
TP128 TPAD28
TP129 TPAD28
TP130 TPAD28
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Title
ICH8M-POWER (4/4)
Size A3
Document Number
Siberia
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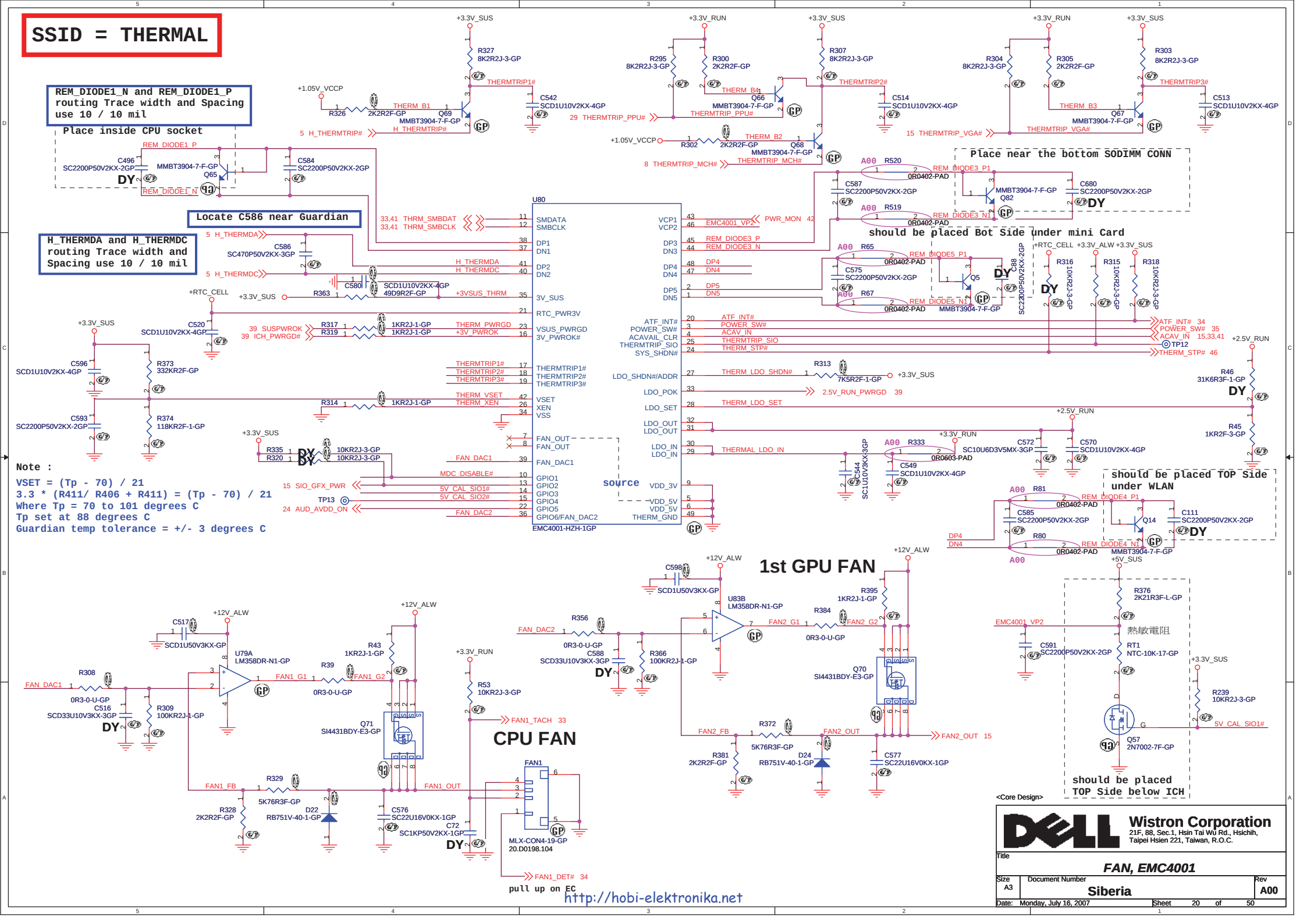
SSID = THERMAL
REM_DIODE1_N and REM_DIODE1_P routing Trace width and Spacing use 10 / 10 mil
Place inside CPU socket
Locate C586 near Guardian
H_THERMDA and H_THERMDC routing Trace width and Spacing use 10 / 10 mil
Place near the bottom SODIMM CONN
should be placed Bot Side under mini Card
should be placed TOP Side under WLAN
should be placed TOP Side below ICH
U80
EMC4001-HZH-1GP
source
1st GPU FAN
CPU FAN
pull up on EC
Note :
VSET = (Tp - 70) / 21
3.3 * (R411/ R406 + R411) = (Tp - 70) / 21
Where Tp = 70 to 101 degrees C
Tp set at 88 degrees C
Guardian temp tolerance = +/- 3 degrees C
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Title
FAN, EMC4001
Size A3
Document Number
Siberia
Rev A00
Date: Monday, July 16, 2007
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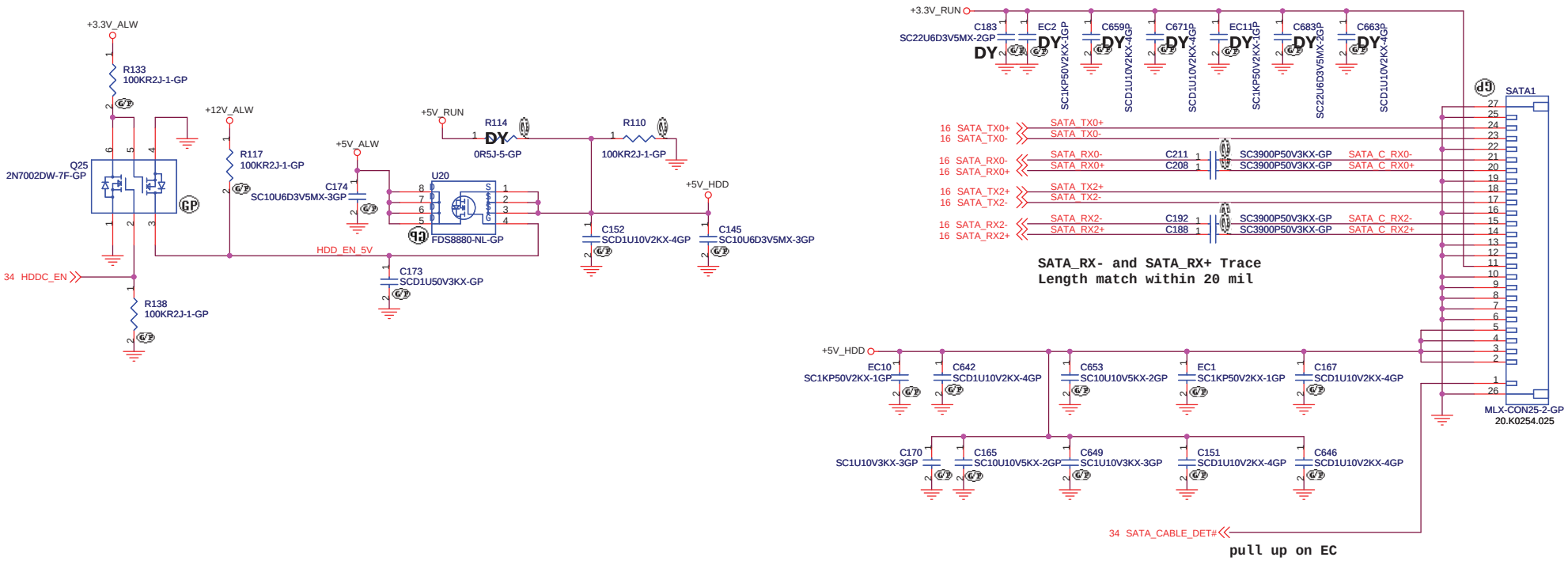
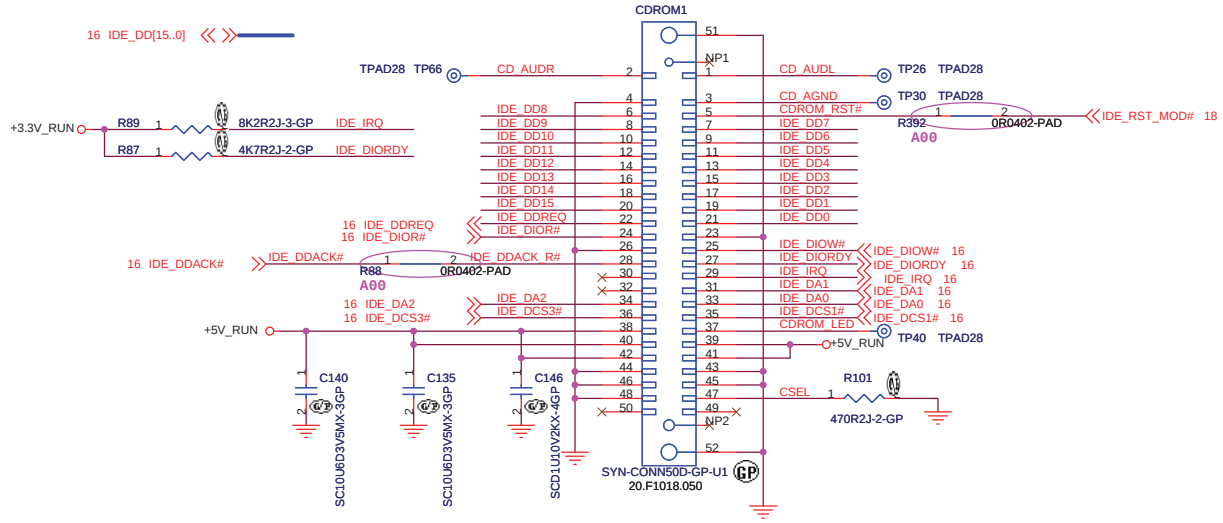
SSID = IDE & SATA

SATA HDD Connector



ODD Connector



<Core Design>

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Title: ***HDD&ODD***

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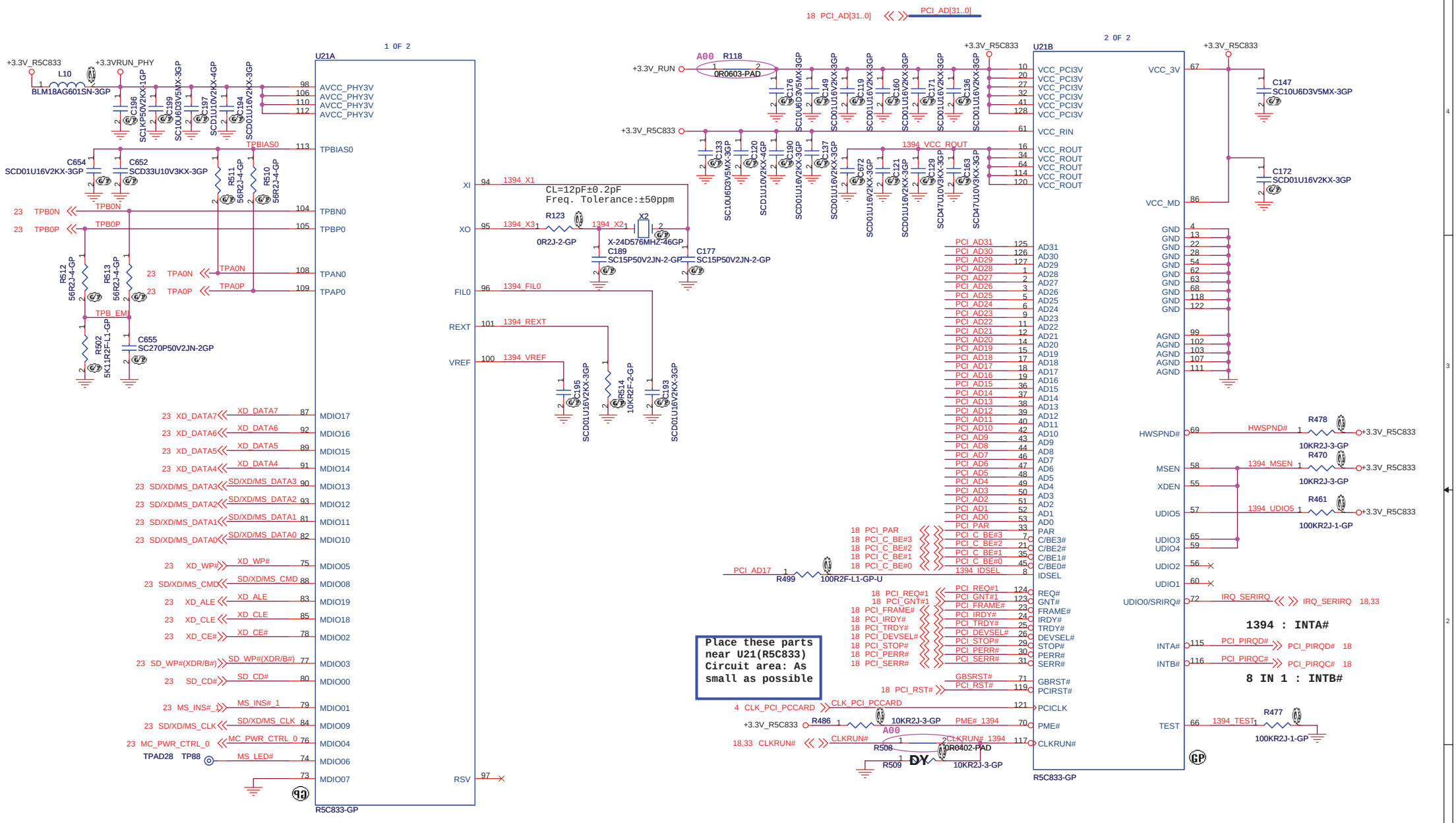
U21A
1 0F 2
R5C833-GP
U21B
2 0F 2
R5C833-GP
+3.3V_R5C833
+3.3VRUN_PHY
+3.3V_RUN
PCI_AD[31..0]
18 PCI_AD[31..0]
CL=12pF±0.2pF
Freq. Tolerance:±50ppm
X-24D576MHZ-46GP
1394 : INTA#
8 IN 1 : INTB#
Place these parts
near U21(R5C833)
Circuit area: As
small as possible
We use the R5C832 in X00 for
R5C833 not ready.
SSID = 1394
EMI
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Title
1394 - R5C833
Size A3
Document Number
Siberia
Rev A00
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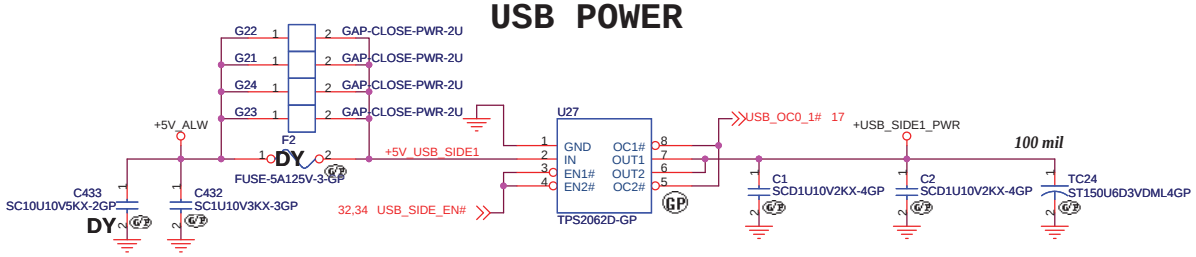
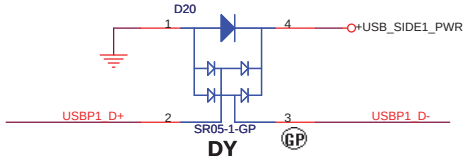
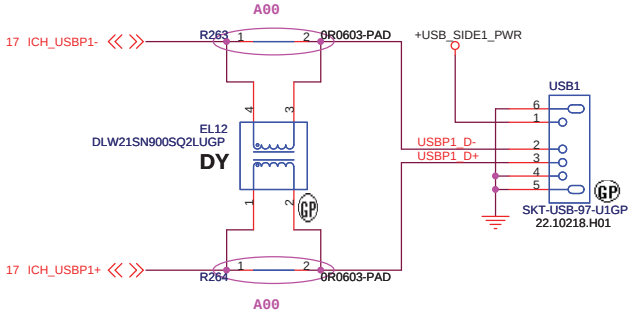
USB POWER



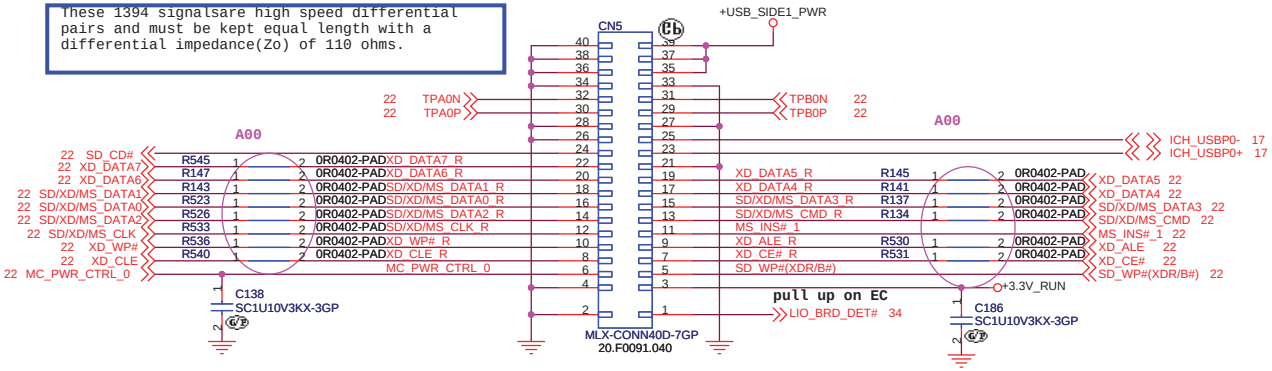


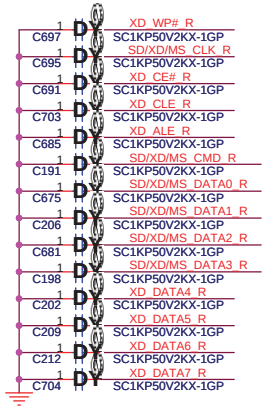
Place ESD diodes as close to the connector as passible.



I/O board conn. (1394/7 IN 1/USB)

These 1394 signalsare high speed differential pairs and must be kept equal length with a differential impedance(Zo) of 110 ohms.





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<Core Design>

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Title	I/O board (1394/7 IN 1/USB) / USB CONN.	
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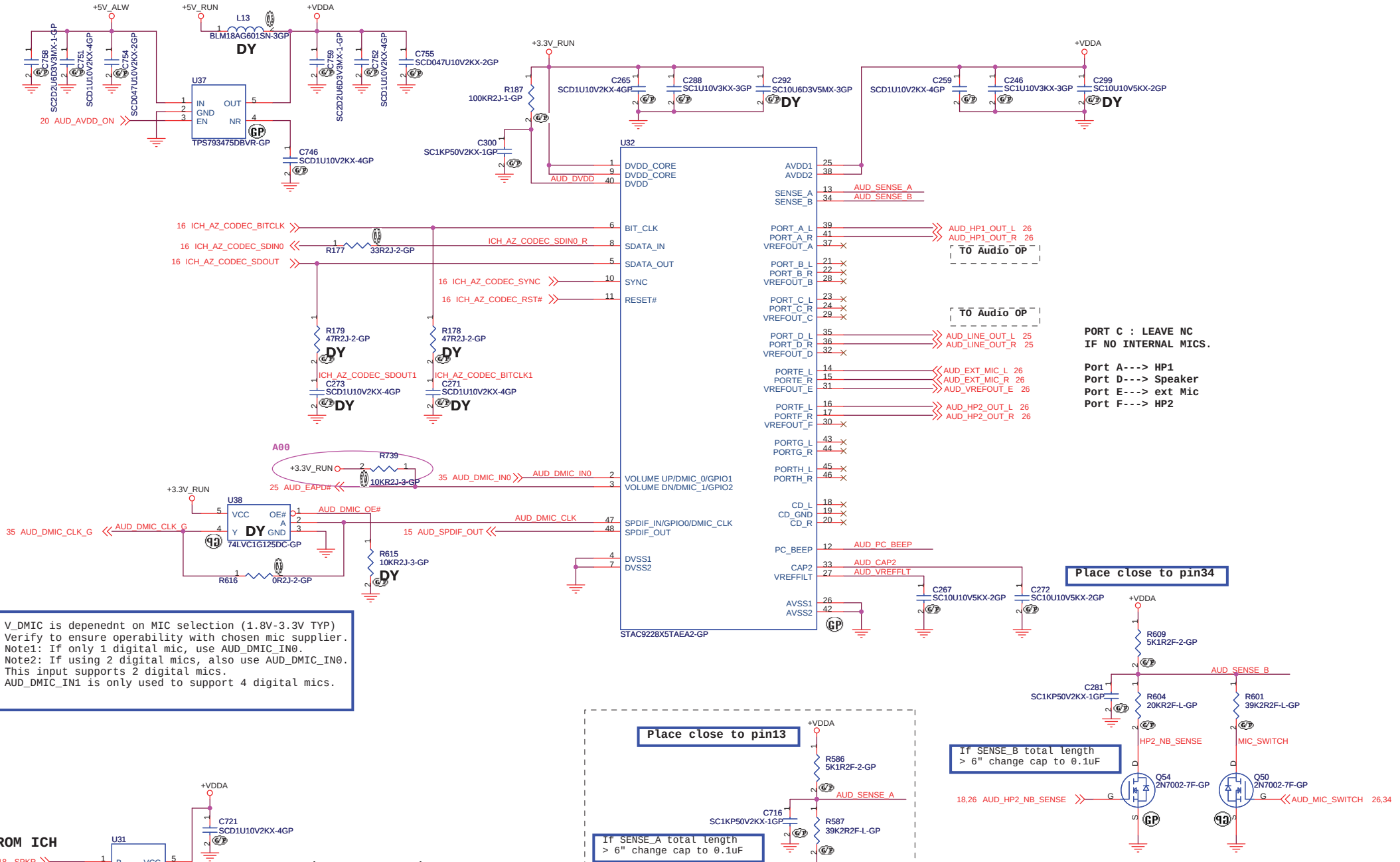

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO (1/3)**

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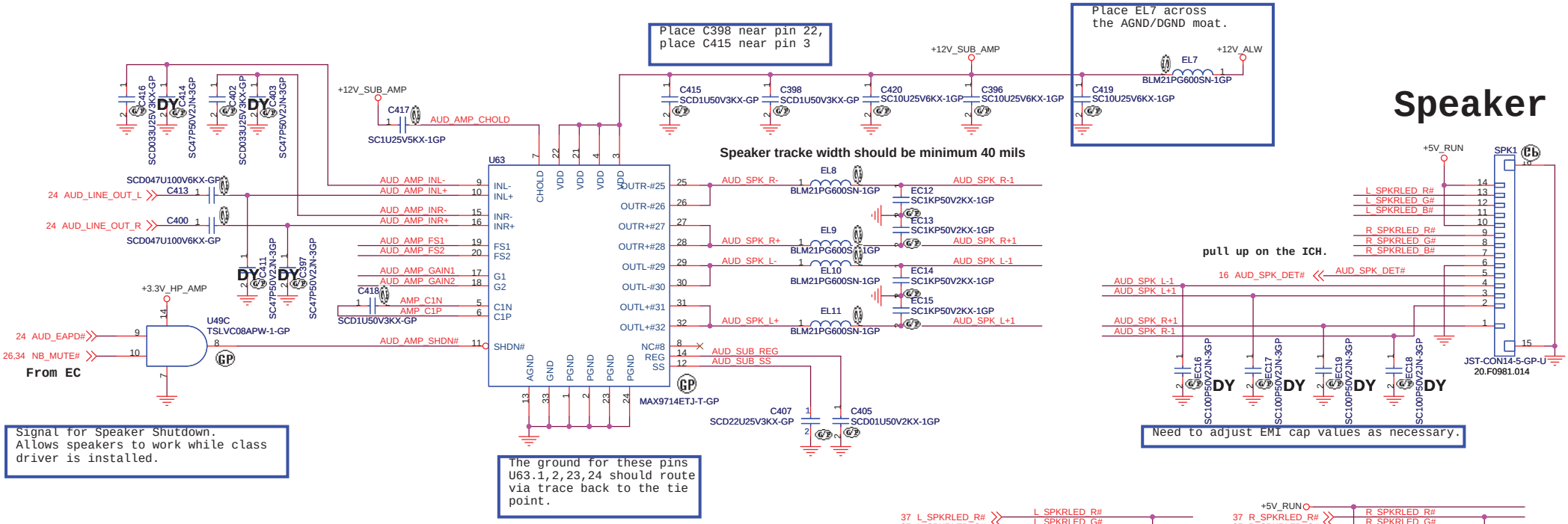

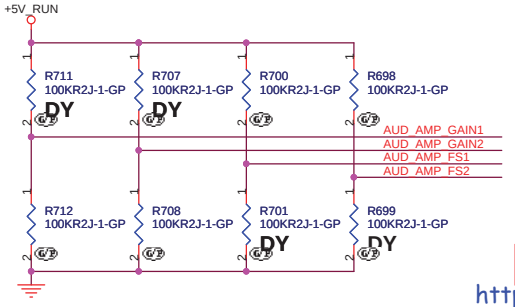

Oscillator freuency selection

FS1	FS2	Freq KHz
0	0	335
0	1	460
1	0	236
1	1	335+/-7% (ss mode)

Voltage Gain selection

G1	G2	AV dB	Input Impedance
0	0	22.1dB	31K ohm
0	1	19.1dB	39K ohm
1	0	13dB	58K ohm
1	1	16dB	48K ohm

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Title: AUDIO (2/3)

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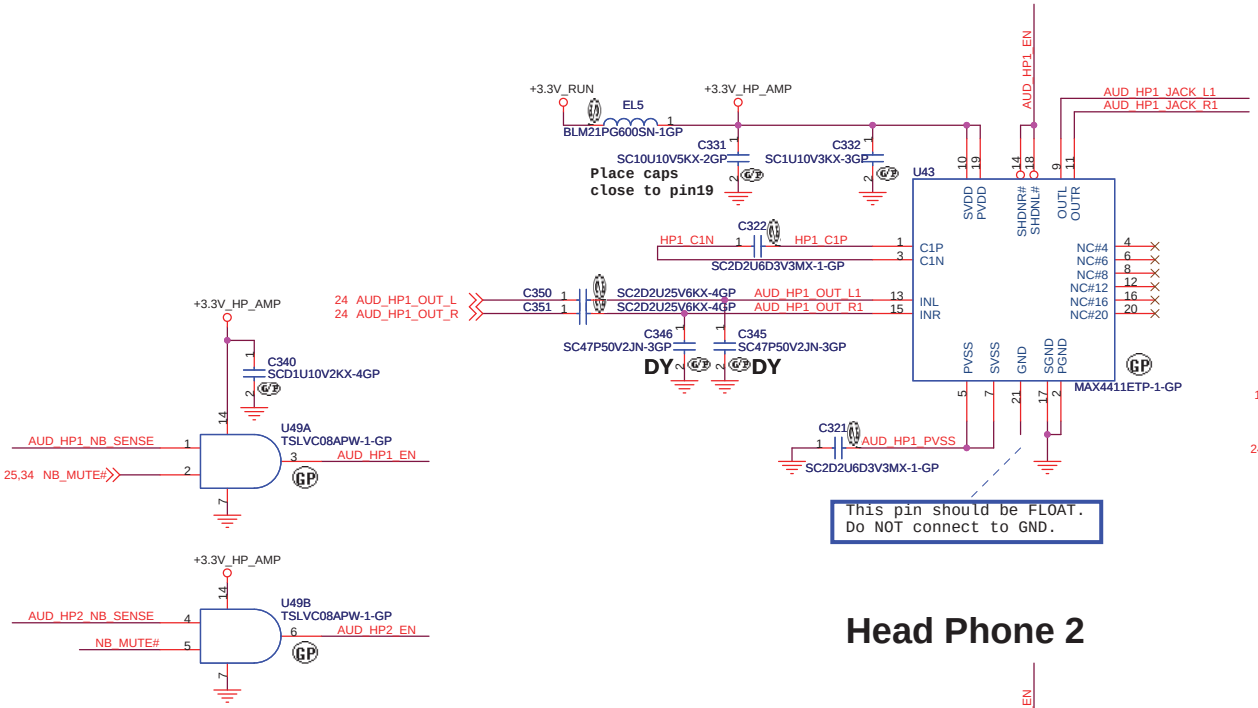
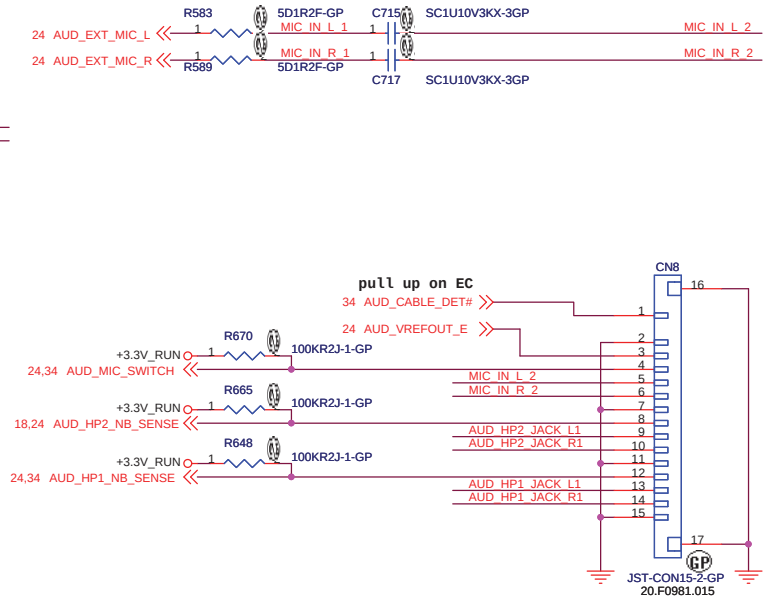
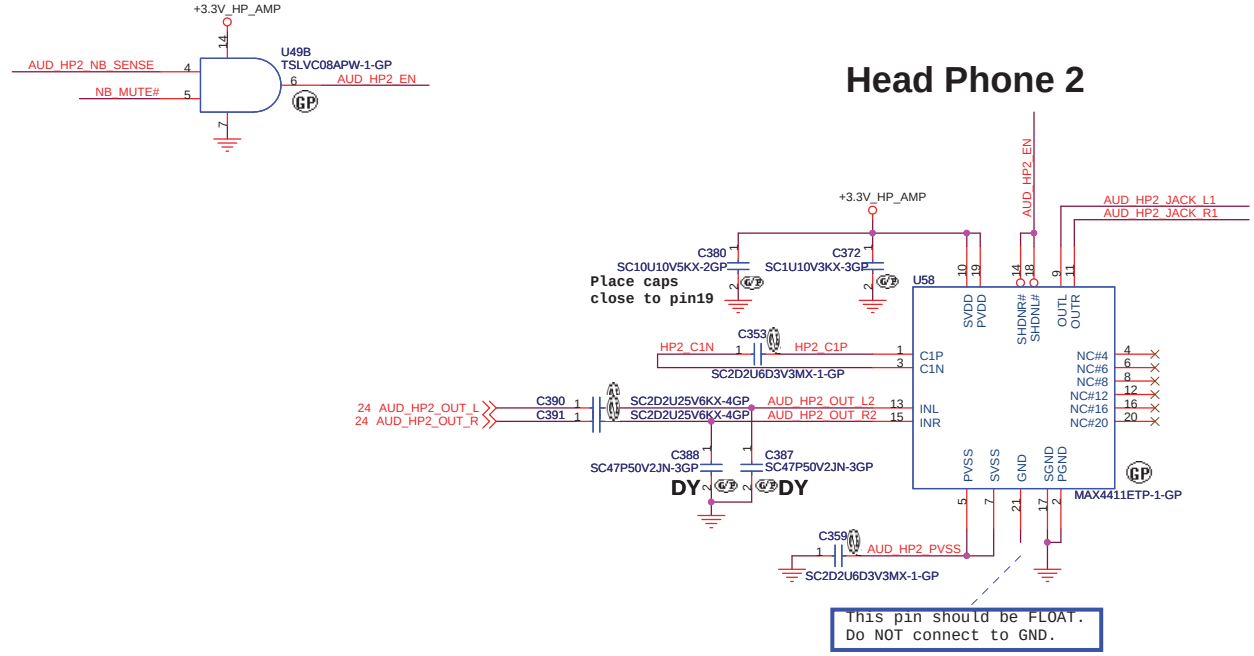
Head Phone 1



MIC



Head Phone 2



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<Core Design>

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Title: AUDIO (3/3)

Size	Document Number	Rev
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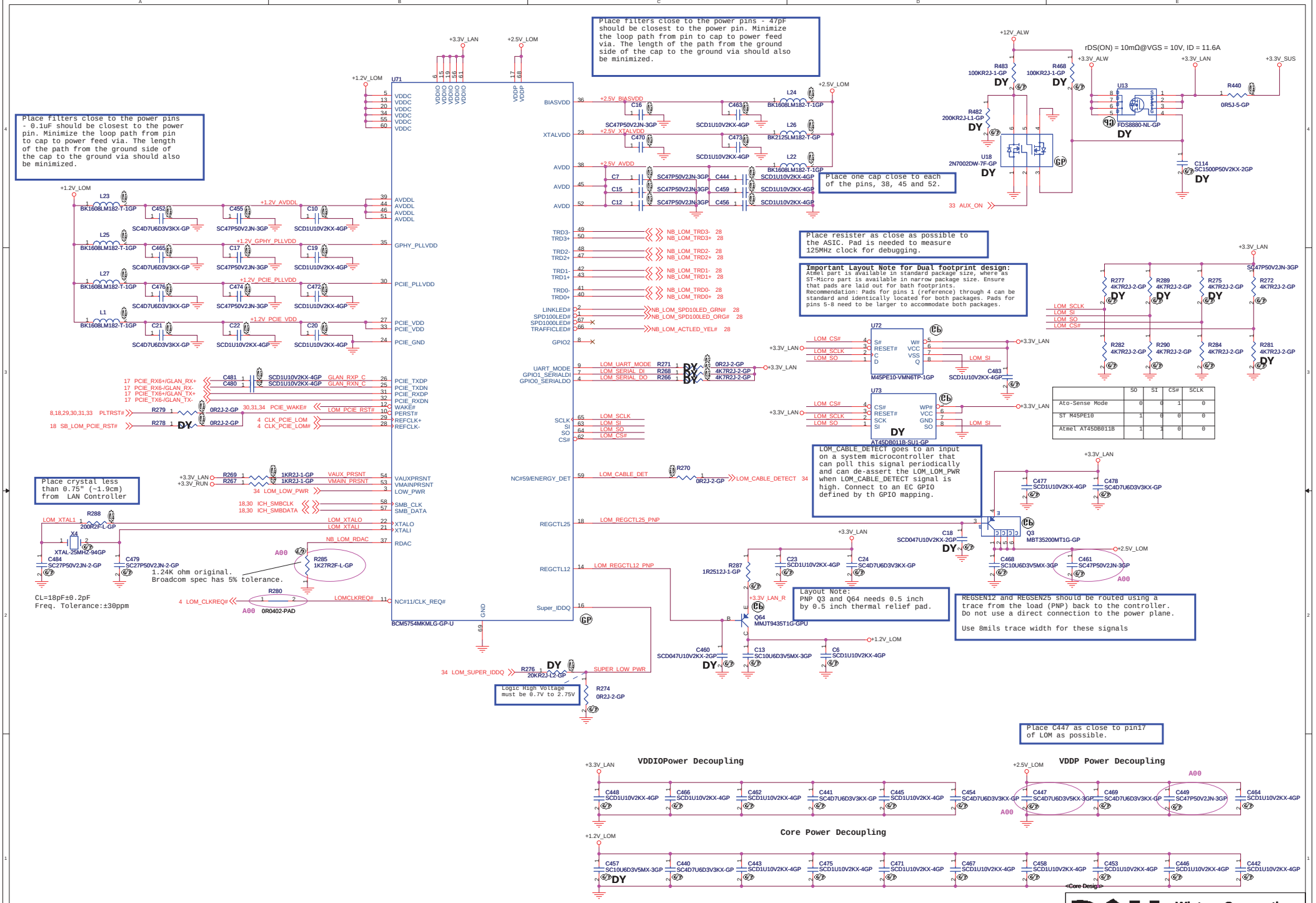
Place filters close to the power pins - 47pF should be closest to the power pin. Minimize the loop path from pin to cap to power feed via. The length of the path from the ground side of the cap to the ground via should also be minimized.
Place filters close to the power pins - 0.1uF should be closest to the power pin. Minimize the loop path from pin to cap to power feed via. The length of the path from the ground side of the cap to the ground via should also be minimized.
Place one cap close to each of the pins, 38, 45 and 52.
Place resister as close as possible to the ASIC. Pad is needed to measure 125MHz clock for debugging.
Important Layout Note for Dual footprint design:
Atmel part is available in standard package size, where as ST-Micro part is available in narrow package size. Ensure that pads are laid out for bath footprints.
Recommendation: Pads for pins 1 (reference) through 4 can be standard and identically located for both packages. Pads for pins 5-8 need to be larger to accommodate both packages.
rDS(ON) = 10mΩ@VGS = 10V, ID = 11.6A
LOM_CABLE_DETECT goes to an input on a system microcontroller that can poll this signal periodically and can de-assert the LOM_LOM_PWR when LOM_CABLE_DETECT signal is high. Connect to an EC GPIO defined by th GPIO mapping.
Place crystal less than 0.75" (~1.9cm) from LAN Controller
CL=18pF±0.2pF
Freq. Tolerance:±30ppm
1.24K ohm original.
Broadcom spec has 5% tolerance.
Logic High Voltage must be 0.7V to 2.75V
Layout Note:
PNP Q3 and Q64 needs 0.5 inch by 0.5 inch thermal relief pad.
REGSEN12 and REGSEN25 should be routed using a trace from the load (PNP) back to the controller. Do not use a direct connection to the power plane.
Use 8mils trace width for these signals
Place C447 as close to pin17 of LOM as possible.
VDDIOPower Decoupling
VDDP Power Decoupling
Core Power Decoupling
Place C457 as close to pin13 of LOM as possible.
Place high-freqency decoupling cpas close to the power pin. Minimize the loop path from pin to cap to power feed via. The length of the path from the ground side ofthe cap to the ground via should also be minimized.
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Title
LAN BCM5754M
Size C
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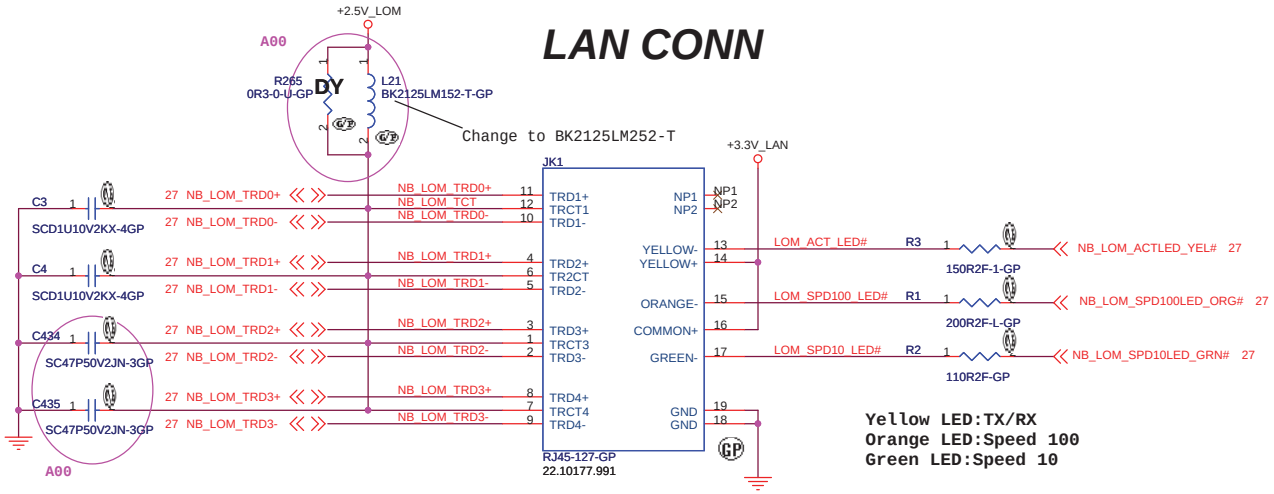
LAN CONN



1. Route as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. Pairs must be equal lengths.
5. 4mil trace width,7mil separation.
6. 30mil between pairs and any other trace.
7. Must not cross ground moat,except RJ-45 moat.

The blowout from the LAN magnetics to the RJ45 connector maintining the distance between the two to be within 1 inch.

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Title: LAN Connector

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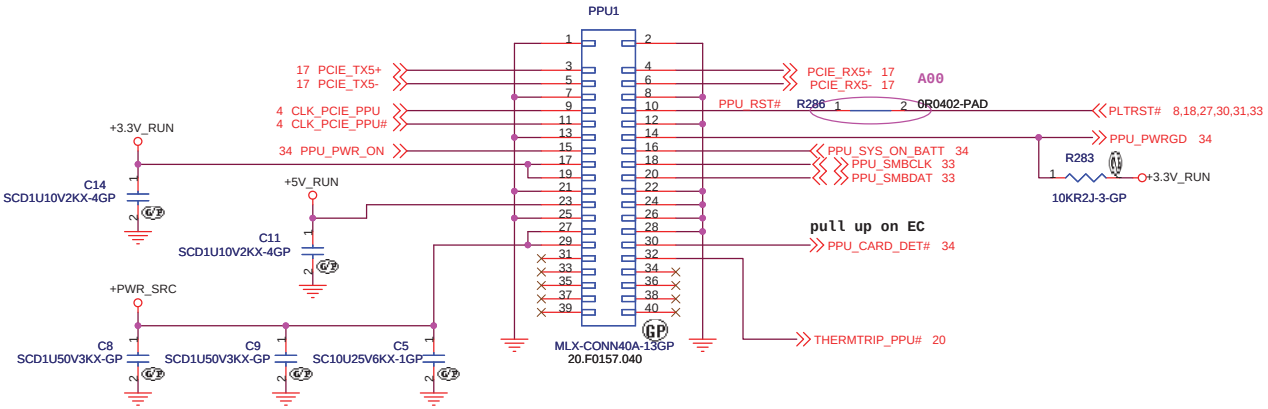
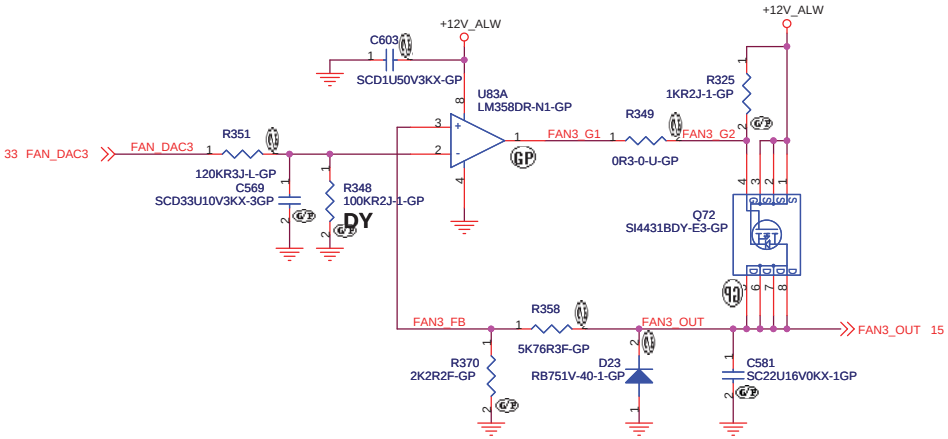
PPU connector



2nd GPU FAN



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Title: PPU CONN. / 2rd GPU FAN

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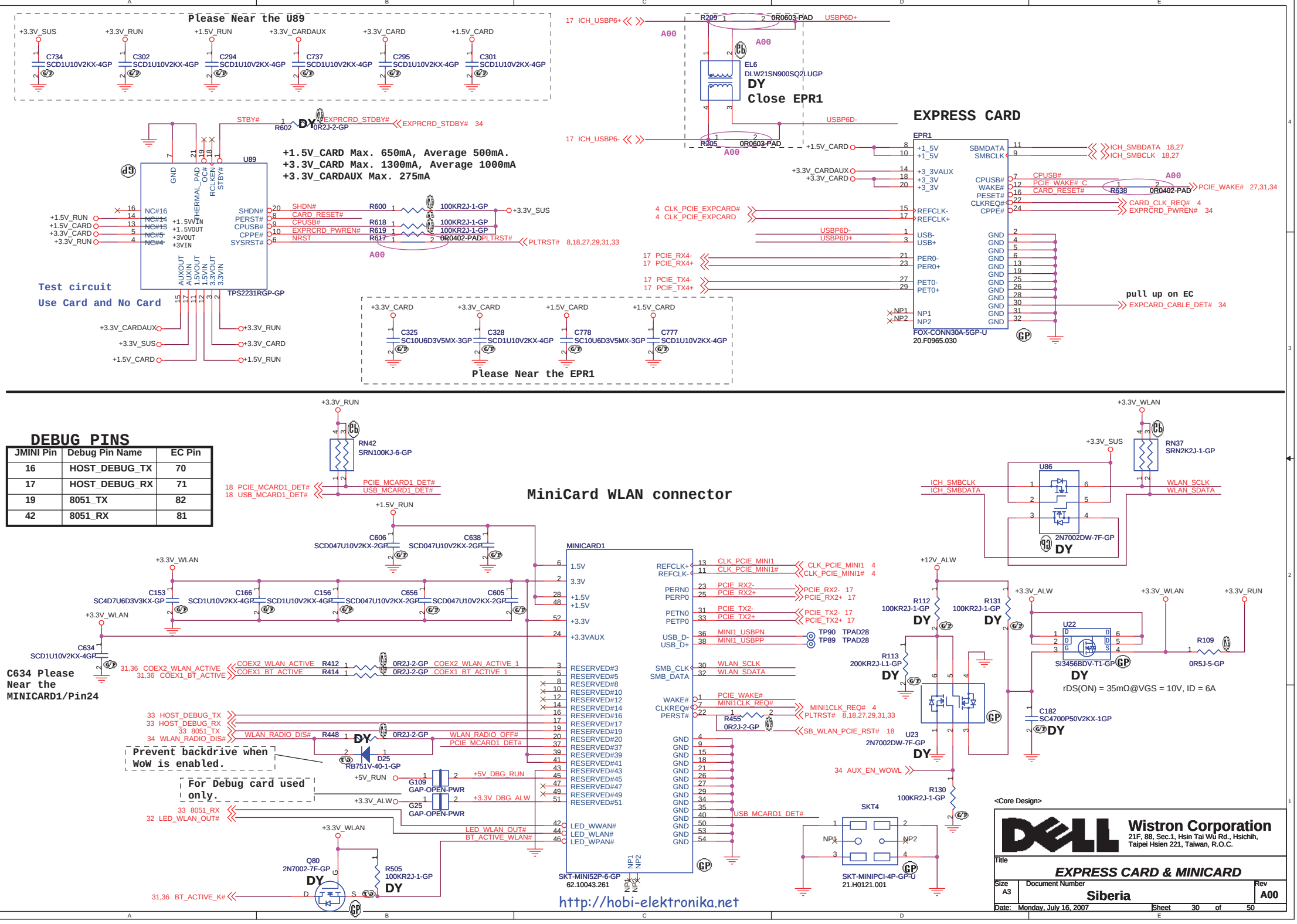
Please Near the U89
+3.3V_SUS
+3.3V_RUN
+1.5V_RUN
+3.3V_CARDAUX
+3.3V_CARD
+1.5V_CARD
C734 SCD1U10V2KX-4GP
C302 SCD1U10V2KX-4GP
C294 SCD1U10V2KX-4GP
C737 SCD1U10V2KX-4GP
C295 SCD1U10V2KX-4GP
C301 SCD1U10V2KX-4GP
17 ICH_USBP6+
R209 0R0603-PAD
USBP6D+
A00
EL6
DLW21SN900SQ2LUGP
DY
Close EPR1
USBP6D-
17 ICH_USBP6-
R205 0R0603-PAD
EXPRESS CARD
EPR1
STBY#
R602 0R2J-2-GP
EXPRCRD_STDBY#
EXPRCRD_STDBY# 34
U89
+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA
TPS2231RGP-GP
SHDN#
PERST#
CPUSB#
CPPE#
SYSRST#
SHDN#
CARD_RESET#
CPUSB#
EXPRCRD_PWREN#
NRST
R600 100KR2J-1-GP
R618 100KR2J-1-GP
R619 100KR2J-1-GP
R617 0R0402-PAD
PLTRST#
PLTRST# 8,18,27,29,31,33
+3.3V_SUS
Test circuit
Use Card and No Card
+3.3V_CARDAUX
+3.3V_SUS
+1.5V_CARD
+3.3V_RUN
+3.3V_CARD
+1.5V_RUN
+3.3V_CARD
+3.3V_CARD
+1.5V_CARD
+1.5V_CARD
C325 SC10U6D3V5MX-3GP
C328 SCD1U10V2KX-4GP
C778 SC10U6D3V5MX-3GP
C777 SCD1U10V2KX-4GP
Please Near the EPR1
+1.5V_CARD
+3.3V_CARDAUX
+3.3V_CARD
4 CLK_PCIE_EXPCARD#
4 CLK_PCIE_EXPCARD
USBP6D-
USBP6D+
17 PCIE_RX4-
17 PCIE_RX4+
17 PCIE_TX4-
17 PCIE_TX4+
ICH_SMBDATA 18,27
ICH_SMBCLK 18,27
CPUSB#
PCIE_WAKE# C
CARD_RESET#
R638 0R0402-PAD
PCIE_WAKE# 27,31,34
CARD_CLK_REQ# 4
EXPRCRD_PWREN# 34
pull up on EC
EXPCARD_CABLE_DET# 34
FOX-CONN30A-5GP-U
20.F0965.030
DEBUG PINS
JMINI Pin | Debug Pin Name | EC Pin
16 | HOST_DEBUG_TX | 70
17 | HOST_DEBUG_RX | 71
19 | 8051_TX | 82
42 | 8051_RX | 81
MiniCard WLAN connector
+3.3V_RUN
RN42 SRN100KJ-6-GP
18 PCIE_MCARD1_DET#
18 USB_MCARD1_DET#
PCIE_MCARD1_DET#
USB_MCARD1_DET#
+1.5V_RUN
C606 SCD047U10V2KX-2GP
C638 SCD047U10V2KX-2GP
+3.3V_WLAN
C153 SC4D7U6D3V3KX-GP
C166 SCD1U10V2KX-4GP
C156 SCD1U10V2KX-4GP
C656 SCD047U10V2KX-2GP
C605 SCD047U10V2KX-2GP
C634 SCD1U10V2KX-4GP
C634 Please Near the MINICARD1/Pin24
31,36 COEX2_WLAN_ACTIVE
31,36 COEX1_BT_ACTIVE
R412 0R2J-2-GP COEX2_WLAN_ACTIVE_1
R414 0R2J-2-GP COEX1_BT_ACTIVE_1
33 HOST_DEBUG_TX
33 HOST_DEBUG_RX
33 8051_TX
34 WLAN_RADIO_DIS#
WLAN_RADIO_DIS#
R448 0R2J-2-GP
WLAN_RADIO_OFF#
PCIE_MCARD1_DET#
D25 RB751V-40-1-GP
Prevent backdrive when WoW is enabled.
For Debug card used only.
+5V_RUN
G109 GAP-OPEN-PWR
+5V_DBG_RUN
+3.3V_ALW
G25 GAP-OPEN-PWR
+3.3V_DBG_ALW
33 8051_RX
32 LED_WLAN_OUT#
LED_WLAN_OUT#
BT_ACTIVE_WLAN#
+3.3V_WLAN
Q80 2N7002-7F-GP
R505 100KR2J-1-GP
31,36 BT_ACTIVE_K#
MINICARD1
1.5V
3.3V
+1.5V
+1.5V
+3.3V
+3.3VAUX
REFCLK+
REFCLK-
CLK_PCIE_MINI1
CLK_PCIE_MINI1#
CLK_PCIE_MINI1 4
CLK_PCIE_MINI1# 4
PERN0
PERP0
PCIE_RX2-
PCIE_RX2+
PCIE_RX2- 17
PCIE_RX2+ 17
PETN0
PETP0
PCIE_TX2-
PCIE_TX2+
PCIE_TX2- 17
PCIE_TX2+ 17
USB_D-
USB_D+
MINI1_USBPN
MINI1_USBPP
TP90 TPAD28
TP89 TPAD28
SMB_CLK
SMB_DATA
WLAN_SCLK
WLAN_SDATA
WAKE#
CLKREQ#
PERST#
PCIE_WAKE#
MINI1CLK_REQ#
MINI1CLK_REQ# 4
PLTRST# 8,18,27,29,31,33
R455 0R2J-2-GP
SB_WLAN_PCIE_RST# 18
USB_MCARD1_DET#
LED_WWAN#
LED_WLAN#
LED_WPAN#
SKT-MINI52P-6-GP
62.10043.261
http://hobi-elektronika.net
+3.3V_WLAN
RN37 SRN2K2J-1-GP
+3.3V_SUS
U86
ICH_SMBCLK
ICH_SMBDATA
WLAN_SCLK
WLAN_SDATA
2N7002DW-7F-GP
DY
+12V_ALW
R112 100KR2J-1-GP DY
R131 100KR2J-1-GP DY
+3.3V_ALW
+3.3V_WLAN
+3.3V_RUN
U22
R109
0R5J-5-GP
SI3456BDV-T1-GP
DY
rDS(ON) = 35mΩ@VGS = 10V, ID = 6A
R113 200KR2J-L1-GP DY
C182 SC4700P50V2KX-1GP
DY
U23 2N7002DW-7F-GP DY
34 AUX_EN_WOWL
R130 100KR2J-1-GP
SKT4
SKT-MINIPCI-4P-GP-U
21.H0121.001
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
EXPRESS CARD & MINICARD
Size A3
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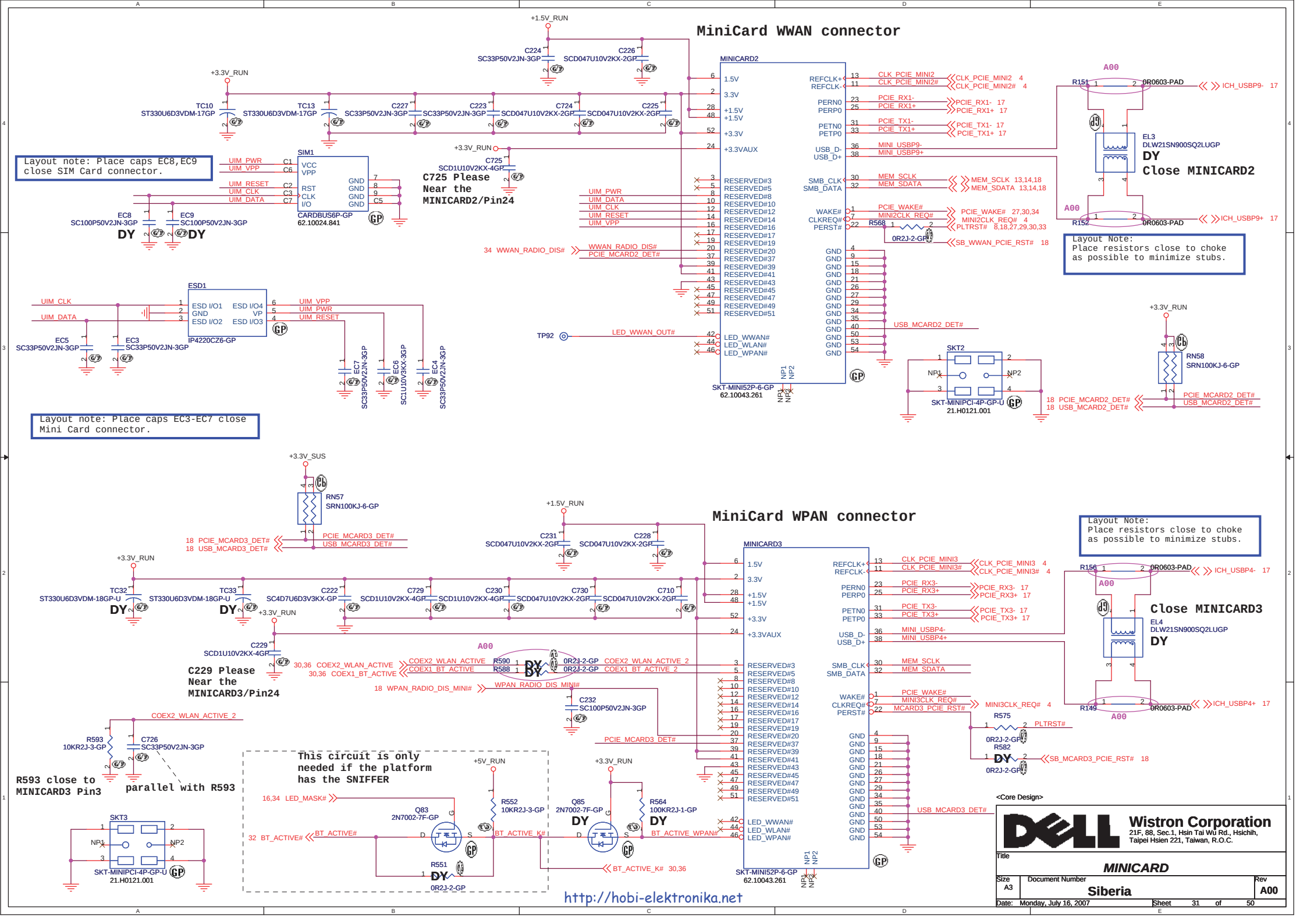
MiniCard WWAN connector
MINICARD2
SKT-MINI52P-6-GP
62.10043.261
SIM1
CARDBUS6P-GP
62.10024.841
ESD1
IP4220CZ6-GP
SKT2
SKT-MINIPCI-4P-GP-U
21.H0121.001
EL3
DLW21SN900SQ2LUGP
DY
Close MINICARD2
Layout note: Place caps EC8,EC9 close SIM Card connector.
C725 Please Near the MINICARD2/Pin24
Layout Note: Place resistors close to choke as possible to minimize stubs.
Layout note: Place caps EC3-EC7 close Mini Card connector.
MiniCard WPAN connector
MINICARD3
SKT-MINI52P-6-GP
62.10043.261
EL4
DLW21SN900SQ2LUGP
Close MINICARD3
C229 Please Near the MINICARD3/Pin24
R593 close to MINICARD3 Pin3
parallel with R593
This circuit is only needed if the platform has the SNIFFER
Q83
2N7002-7F-GP
Q85
2N7002-7F-GP
R552
10KR2J-3-GP
R564
100KR2J-1-GP
R551
0R2J-2-GP
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
MINICARD
Siberia
A00
Date: Monday, July 16, 2007
Sheet 31 of 50
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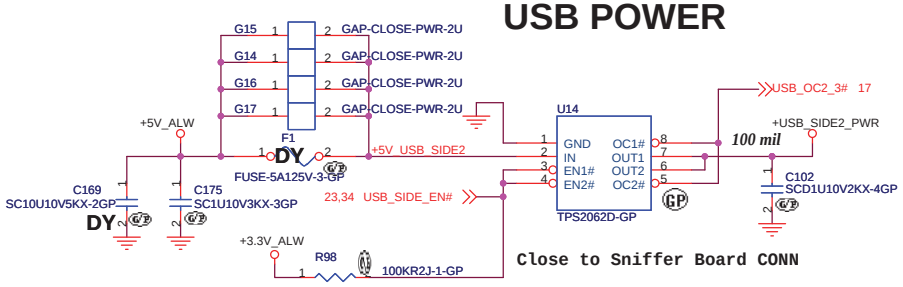
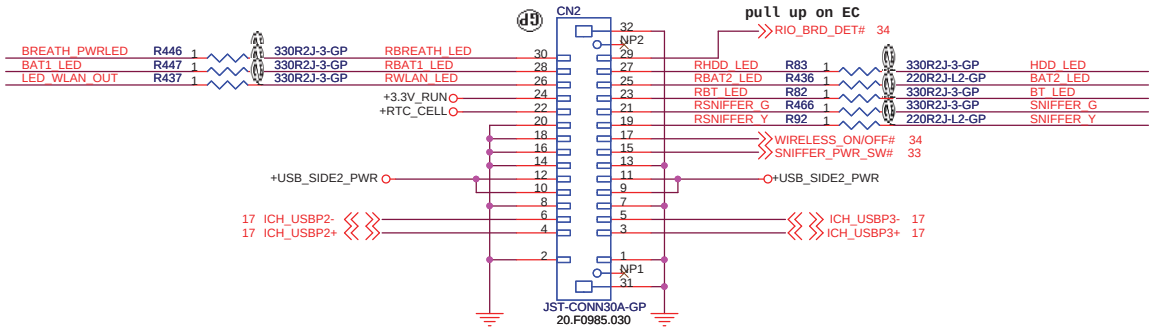
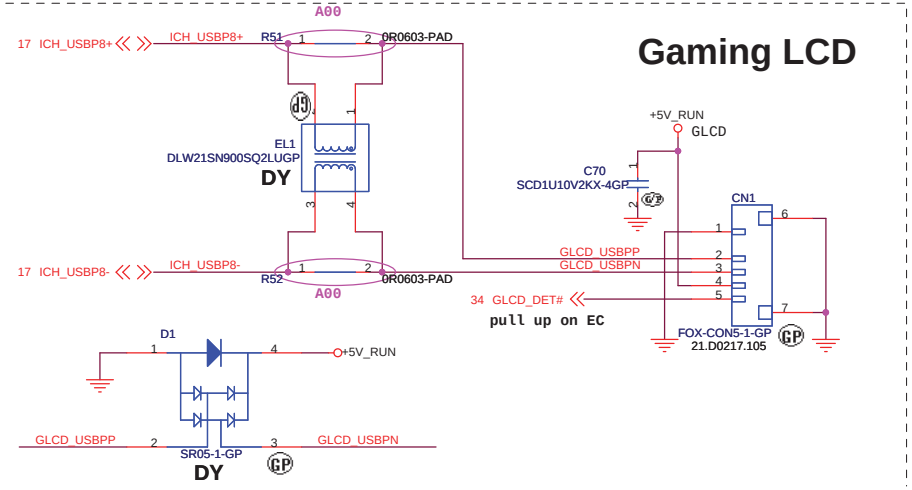
USB POWER



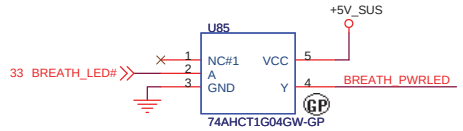
Sniffer board for USB, Indicator LEDs, Sniffer Switch conn.



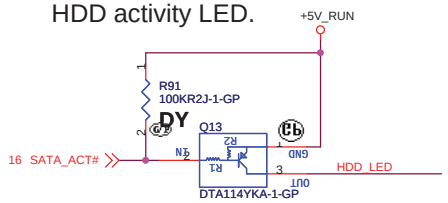
Gaming LCD



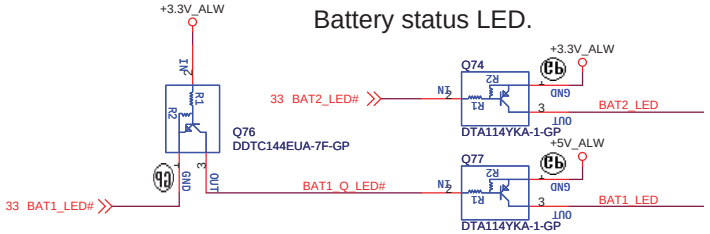
Power & Suspend LED.



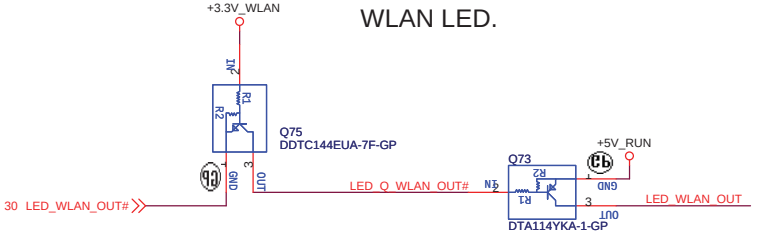
HDD activity LED.



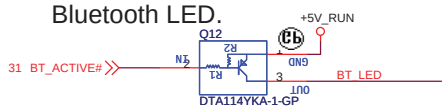
Battery status LED.



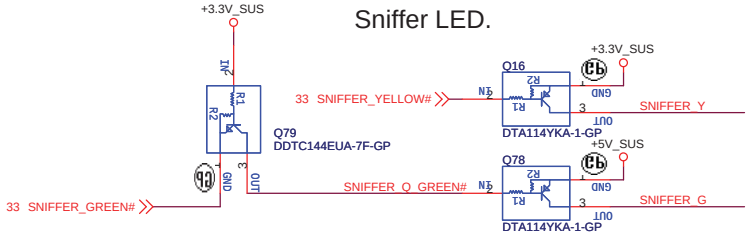
WLAN LED.



Bluetooth LED.



Sniffer LED.



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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Sniffer board (USB/Status LEDs) / Gaming LCD*

Size: A3 | Document Number: **Siberia** | Rev: A00

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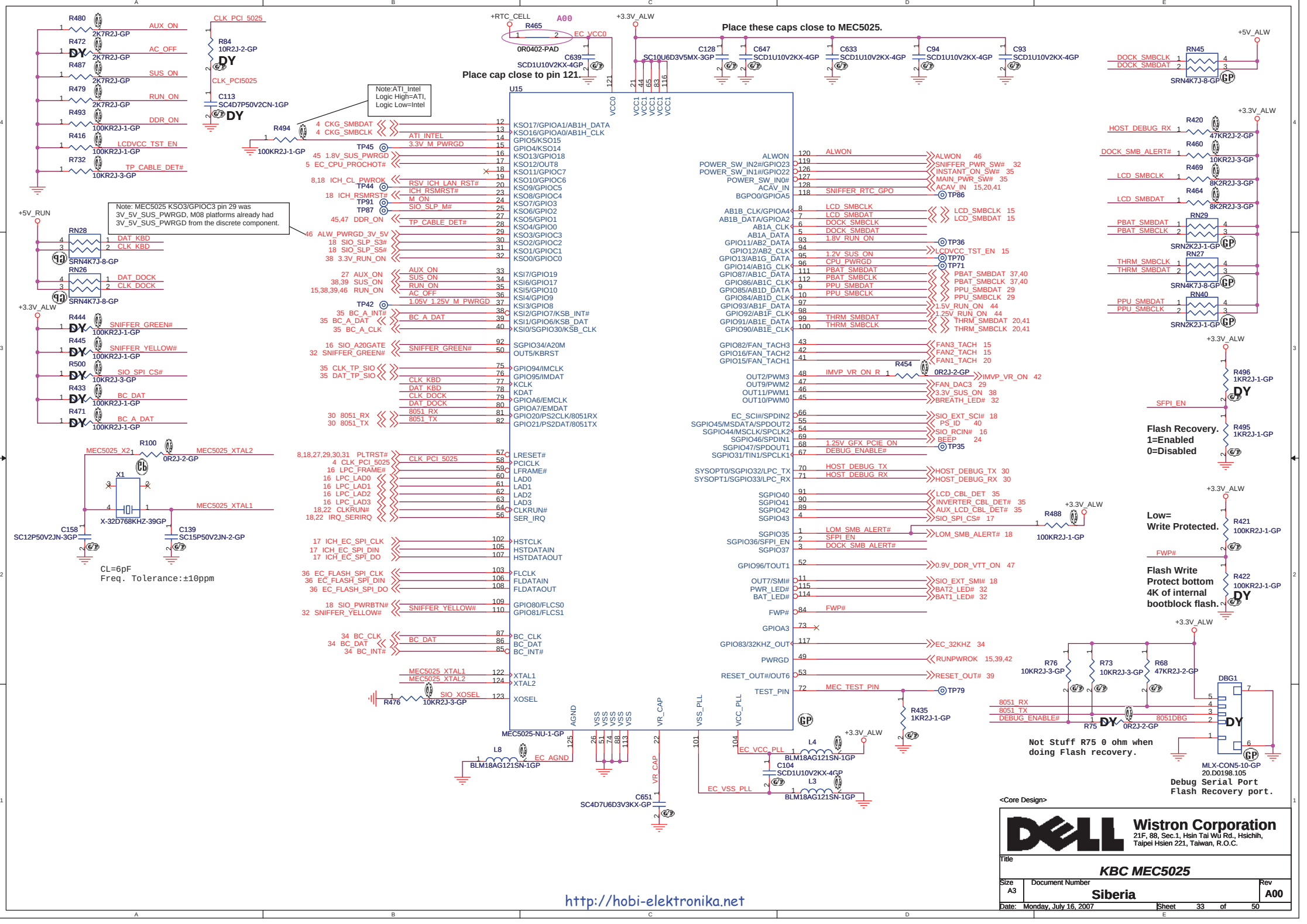
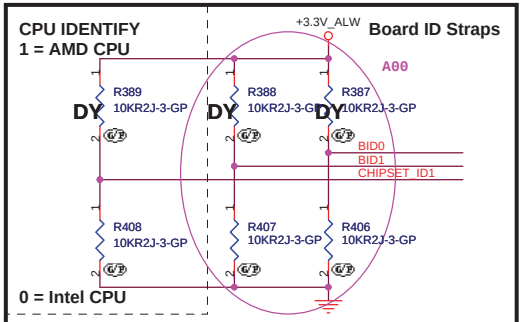
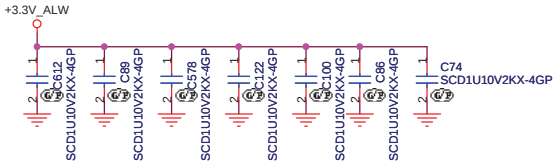
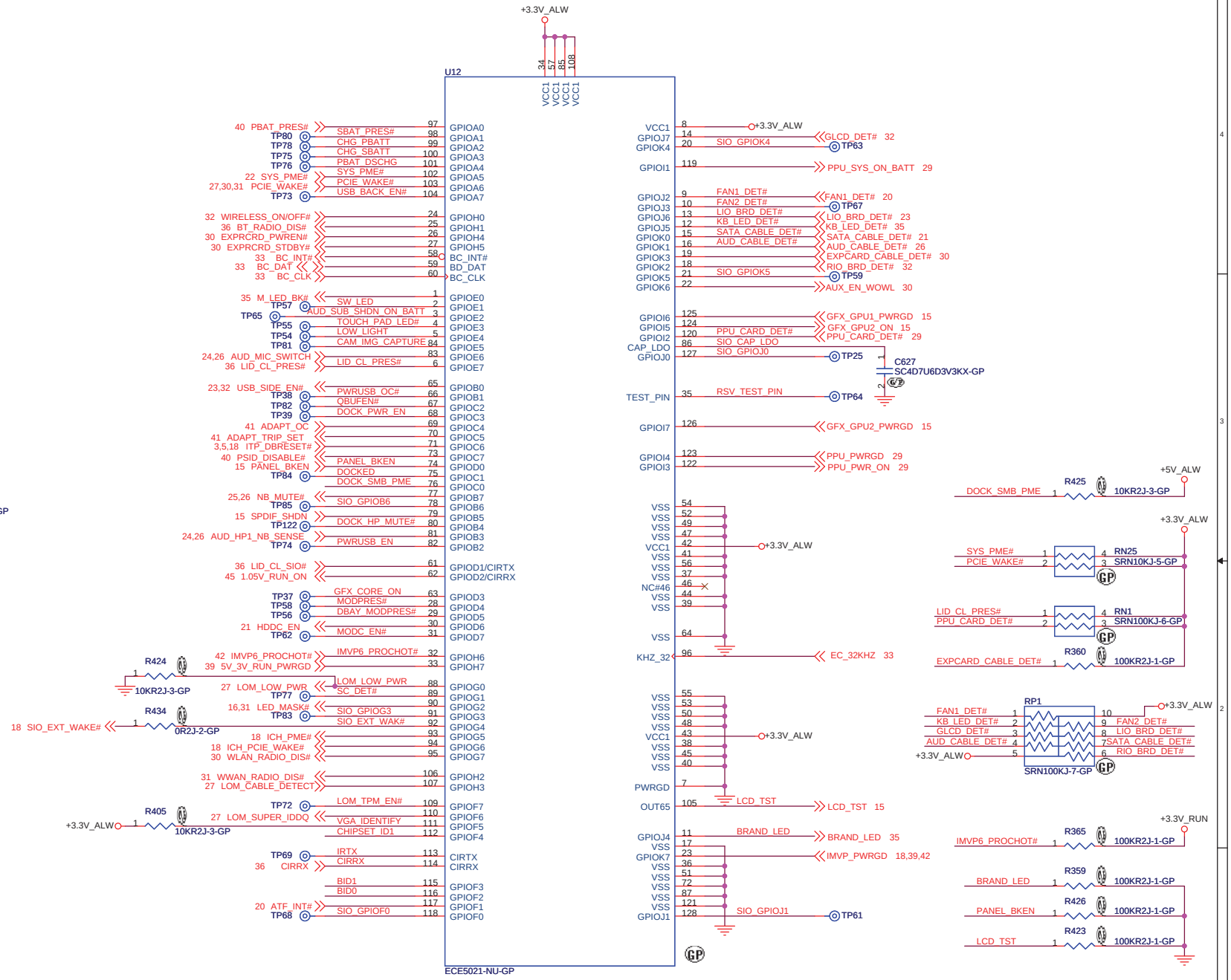


http://hobi-elektronika.net



BID1	BID0	Board Rev.
0	0	ENG1(A00)
0	1	ENG2(X01)
1	0	QT (X02)
1	1	RAMP





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***SIO ECE5021***

Size: A3 | Document Number: **Siberia** | Rev: **A00**

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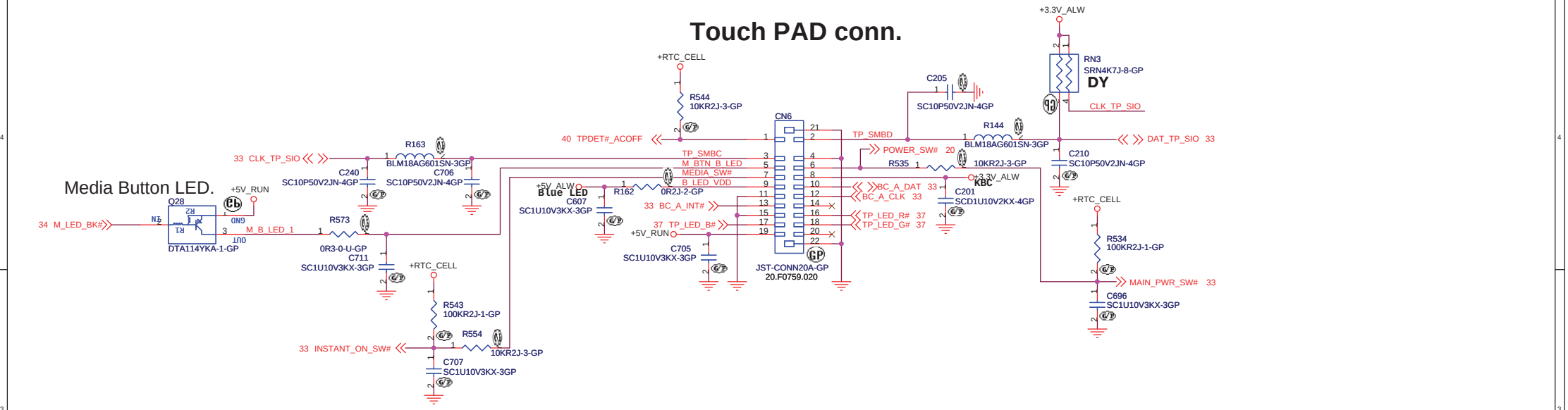
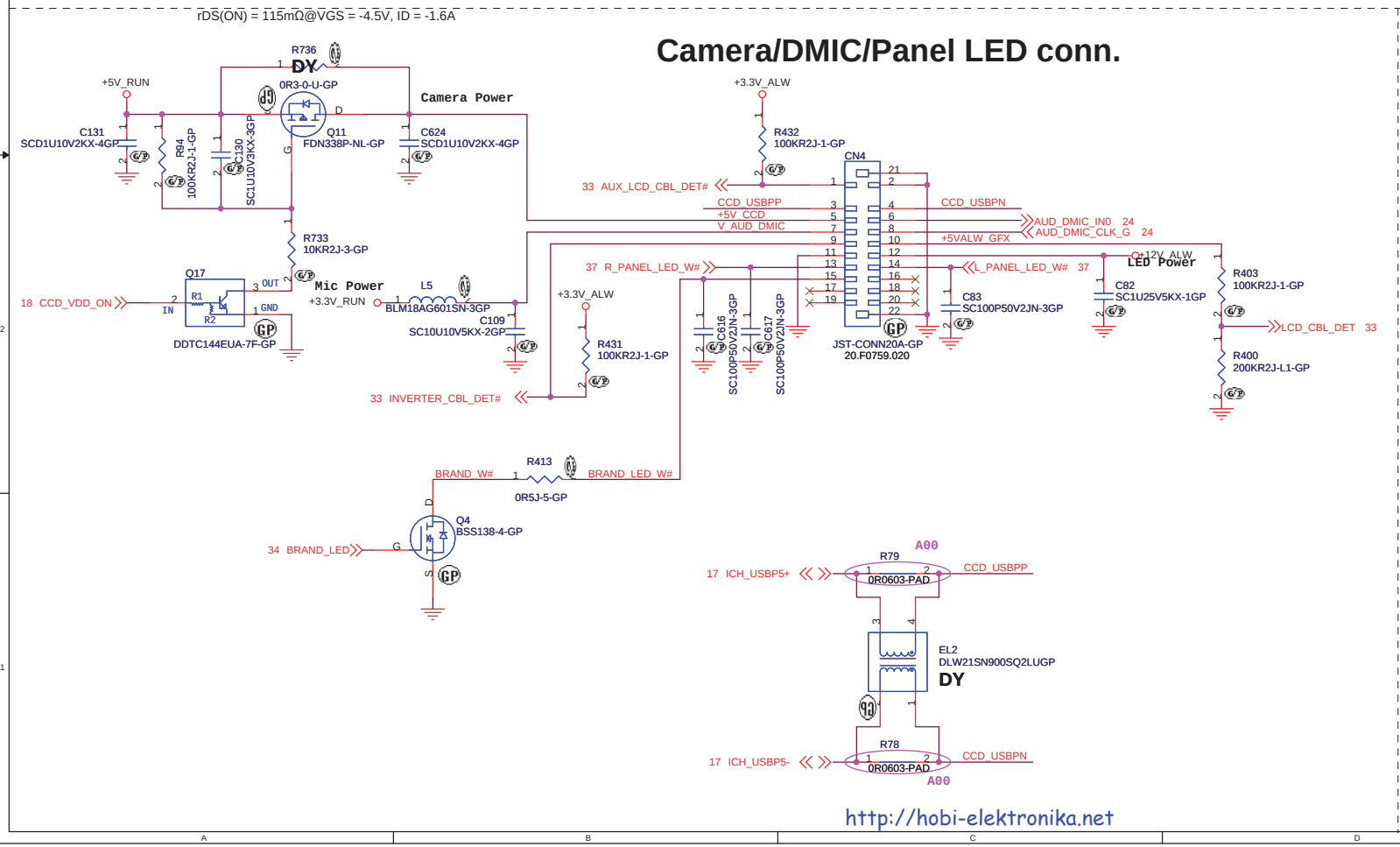
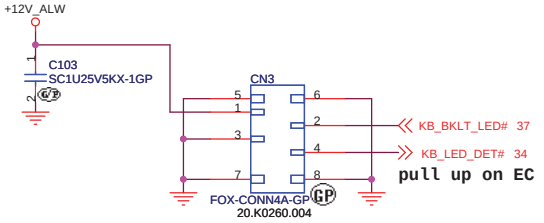
Touch PAD conn.



Camera/DMIC/Panel LED conn.



KB BKLT LED



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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Touch PAD/Camera/DMIC*

Size	Document Number	Rev
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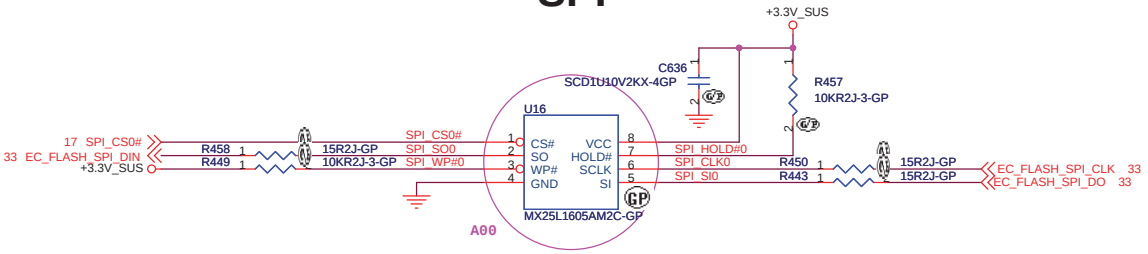
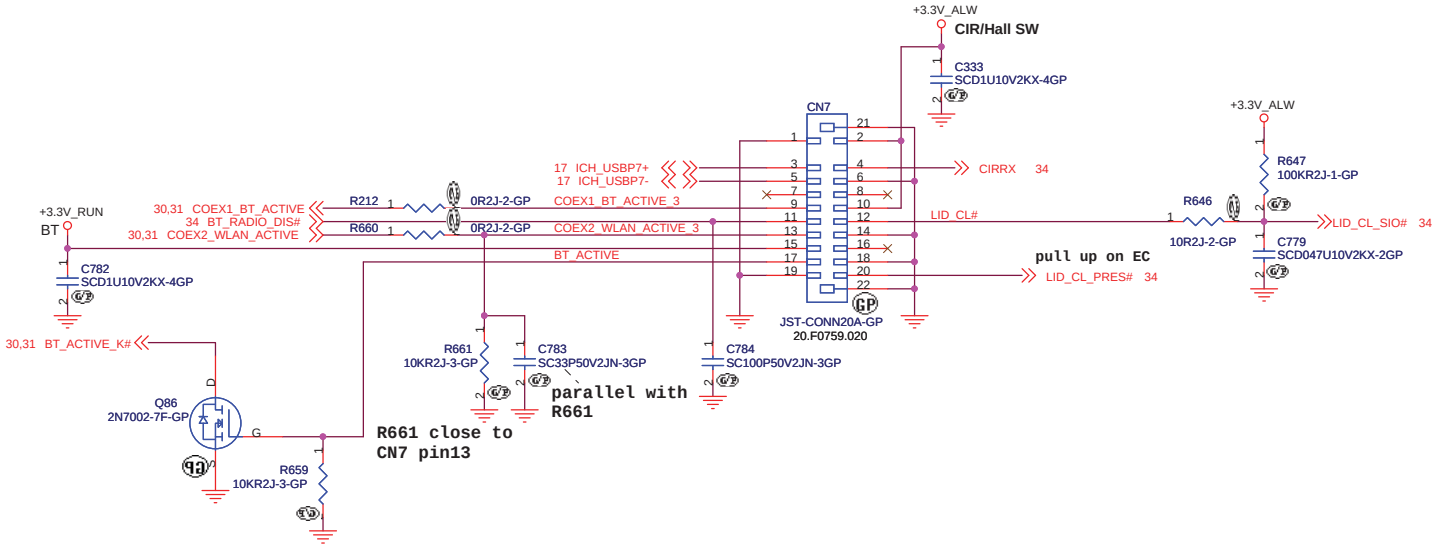
SPI



Bluetooth/ CIR/ Hall SW



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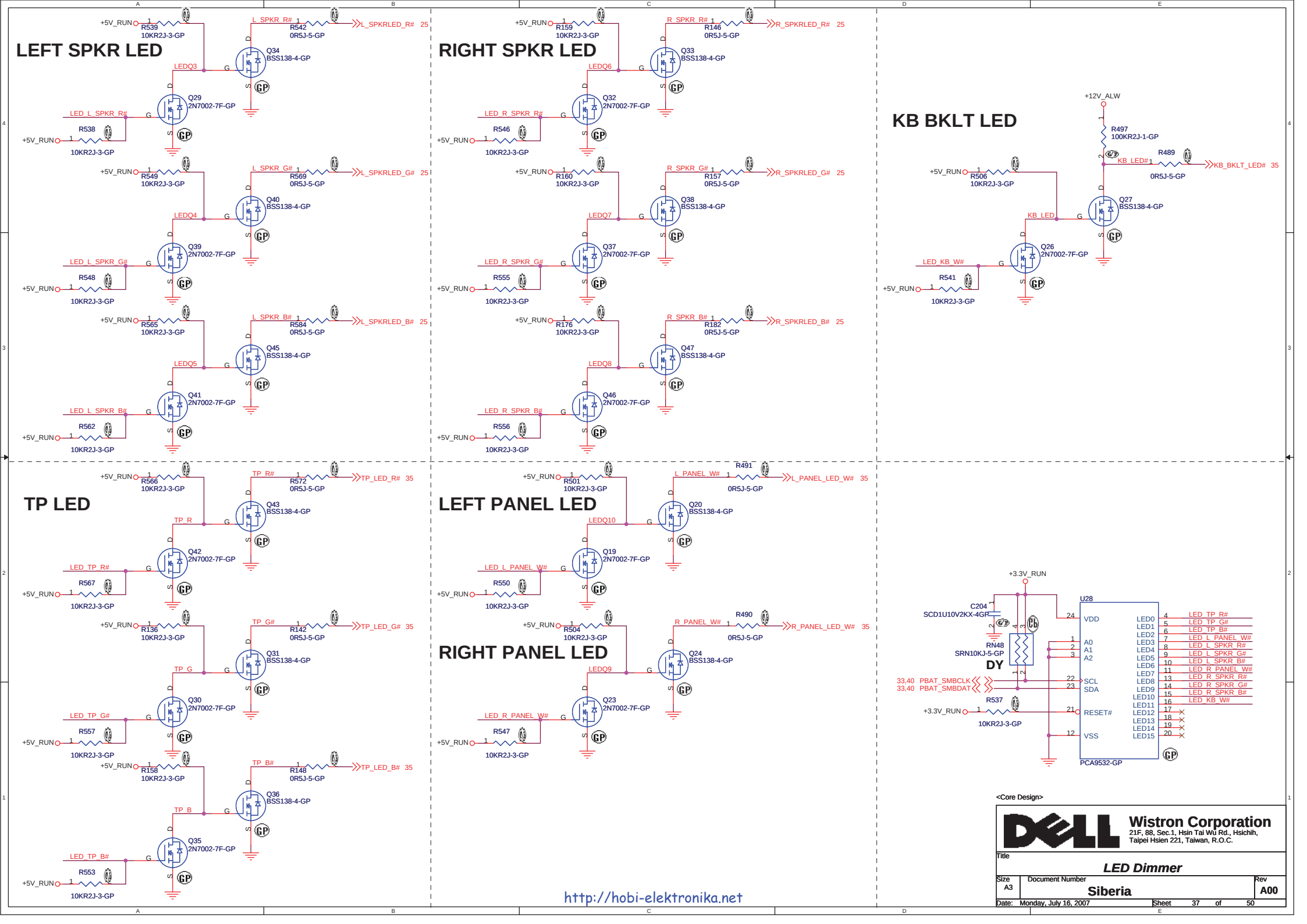
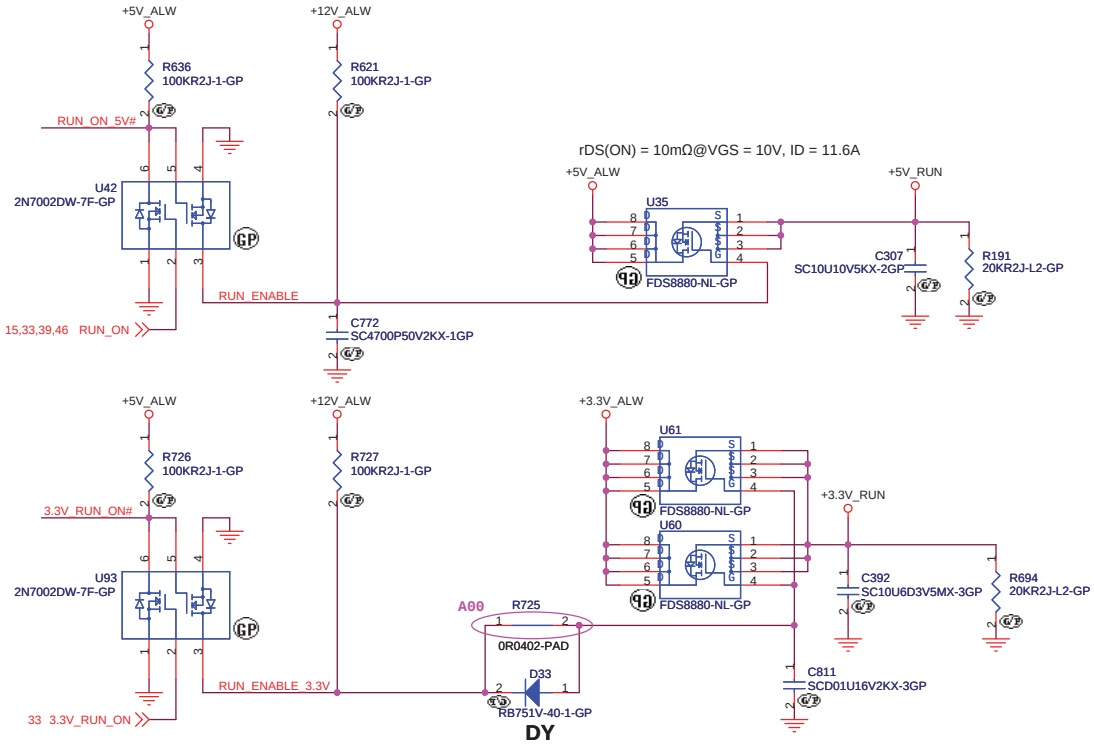
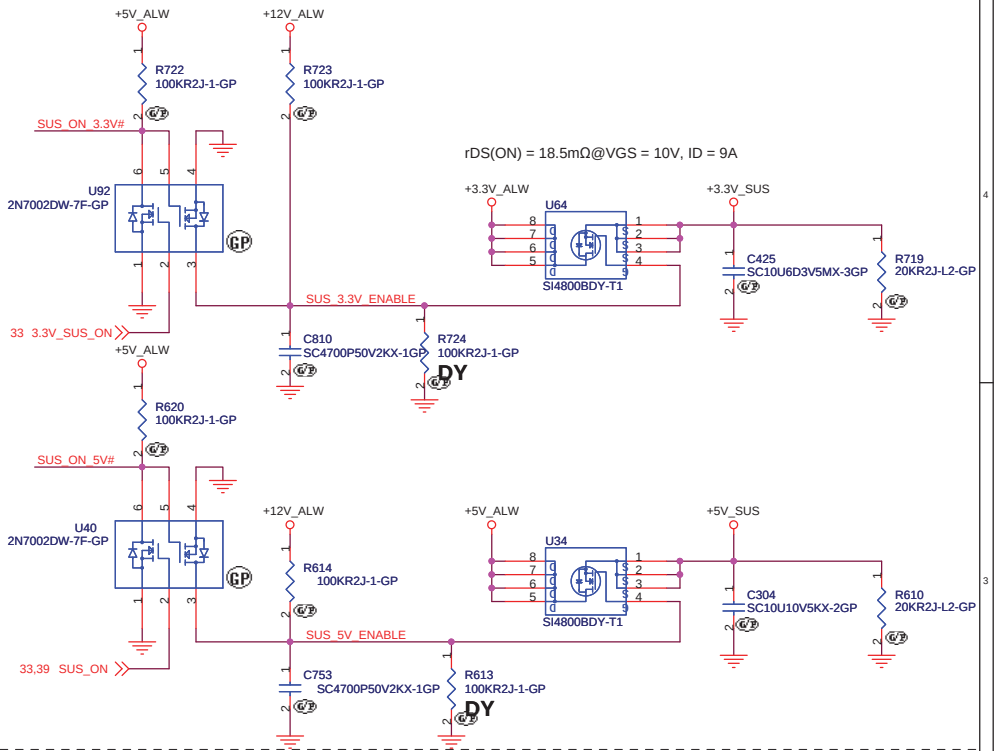
<Core Design>

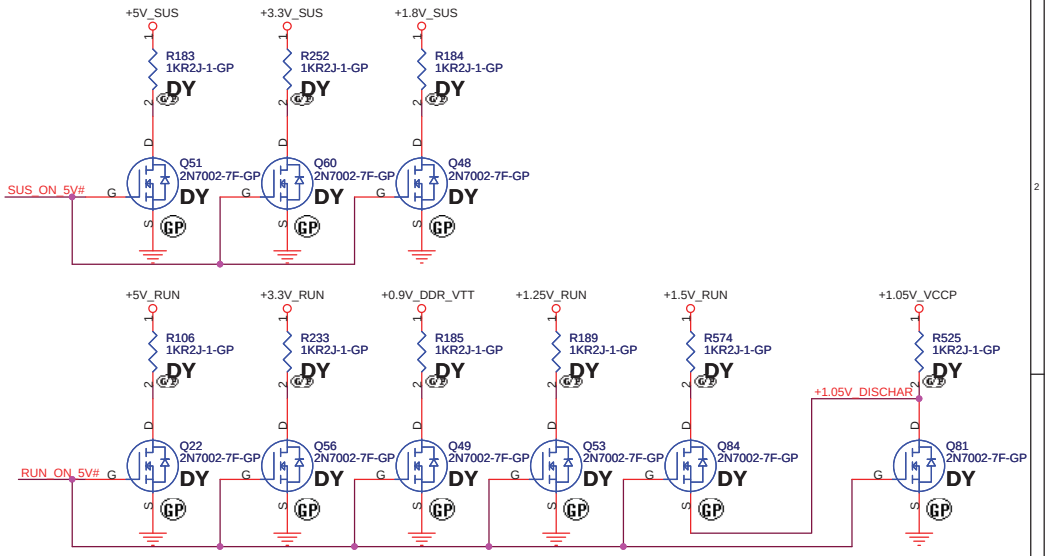
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*SPI FLASH / Bluetooth / CIR / LID*	
Size A3	Document Number **Siberia**	Rev **A00**
Date: Monday, July 16, 2007	Sheet 36 of 50	


LEFT SPKR LED
RIGHT SPKR LED
KB BKLT LED
TP LED
LEFT PANEL LED
RIGHT PANEL LED
+5V_RUN
+12V_ALW
+3.3V_RUN
L_SPKR_R#
R539 10KR2J-3-GP
R542 0R5J-5-GP
L_SPKRLED_R# 25
Q34 BSS138-4-GP
LEDQ3
Q29 2N7002-7F-GP
LED_L_SPKR_R#
R538 10KR2J-3-GP
L_SPKR_G#
R549 10KR2J-3-GP
R569 0R5J-5-GP
L_SPKRLED_G# 25
Q40 BSS138-4-GP
LEDQ4
Q39 2N7002-7F-GP
LED_L_SPKR_G#
R548 10KR2J-3-GP
L_SPKR_B#
R565 10KR2J-3-GP
R584 0R5J-5-GP
L_SPKRLED_B# 25
Q45 BSS138-4-GP
LEDQ5
Q41 2N7002-7F-GP
LED_L_SPKR_B#
R562 10KR2J-3-GP
R_SPKR_R#
R159 10KR2J-3-GP
R146 0R5J-5-GP
R_SPKRLED_R# 25
Q33 BSS138-4-GP
LEDQ6
Q32 2N7002-7F-GP
LED_R_SPKR_R#
R546 10KR2J-3-GP
R_SPKR_G#
R160 10KR2J-3-GP
R157 0R5J-5-GP
R_SPKRLED_G# 25
Q38 BSS138-4-GP
LEDQ7
Q37 2N7002-7F-GP
LED_R_SPKR_G#
R555 10KR2J-3-GP
R_SPKR_B#
R176 10KR2J-3-GP
R182 0R5J-5-GP
R_SPKRLED_B# 25
Q47 BSS138-4-GP
LEDQ8
Q46 2N7002-7F-GP
LED_R_SPKR_B#
R556 10KR2J-3-GP
R497 100KR2J-1-GP
KB_LED#
R489 0R5J-5-GP
KB_BKLT_LED# 35
R506 10KR2J-3-GP
Q27 BSS138-4-GP
KB_LED
Q26 2N7002-7F-GP
LED_KB_W#
R541 10KR2J-3-GP
TP_R#
R566 10KR2J-3-GP
R572 0R5J-5-GP
TP_LED_R# 35
Q43 BSS138-4-GP
TP_R
Q42 2N7002-7F-GP
LED_TP_R#
R567 10KR2J-3-GP
TP_G#
R136 10KR2J-3-GP
R142 0R5J-5-GP
TP_LED_G# 35
Q31 BSS138-4-GP
TP_G
Q30 2N7002-7F-GP
LED_TP_G#
R557 10KR2J-3-GP
TP_B#
R158 10KR2J-3-GP
R148 0R5J-5-GP
TP_LED_B# 35
Q36 BSS138-4-GP
TP_B
Q35 2N7002-7F-GP
LED_TP_B#
R553 10KR2J-3-GP
L_PANEL_W#
R501 10KR2J-3-GP
R491 0R5J-5-GP
L_PANEL_LED_W# 35
Q20 BSS138-4-GP
LEDQ10
Q19 2N7002-7F-GP
LED_L_PANEL_W#
R550 10KR2J-3-GP
R_PANEL_W#
R504 10KR2J-3-GP
R490 0R5J-5-GP
R_PANEL_LED_W# 35
Q24 BSS138-4-GP
LEDQ9
Q23 2N7002-7F-GP
LED_R_PANEL_W#
R547 10KR2J-3-GP
C204 SCD1U10V2KX-4GP
RN48 SRN10KJ-5-GP
DY
U28
VDD
A0
A1
A2
SCL
SDA
RESET#
VSS
PCA9532-GP
33,40 PBAT_SMBCLK
33,40 PBAT_SMBDAT
R537 10KR2J-3-GP
LED0 LED_TP_R#
LED1 LED_TP_G#
LED2 LED_TP_B#
LED3 LED_L_PANEL_W#
LED4 LED_L_SPKR_R#
LED5 LED_L_SPKR_G#
LED6 LED_L_SPKR_B#
LED7 LED_R_PANEL_W#
LED8 LED_R_SPKR_R#
LED9 LED_R_SPKR_G#
LED10 LED_R_SPKR_B#
LED11 LED_KB_W#
LED12
LED13
LED14
LED15
http://hobi-elektronika.net
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
LED Dimmer
Size A3
Document Number
Siberia
Rev A00
Date: Monday, July 16, 2007
Sheet 37 of 50







Reserve discharge path

CRB 0.95:
Insures that +1.05_VCCP and +1.5_RUN ramp down together by discharing +1.5V_RUN into +1.05V_VCCP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Plane Enable***

Size	Document Number	Rev
A3	Siberia	A00

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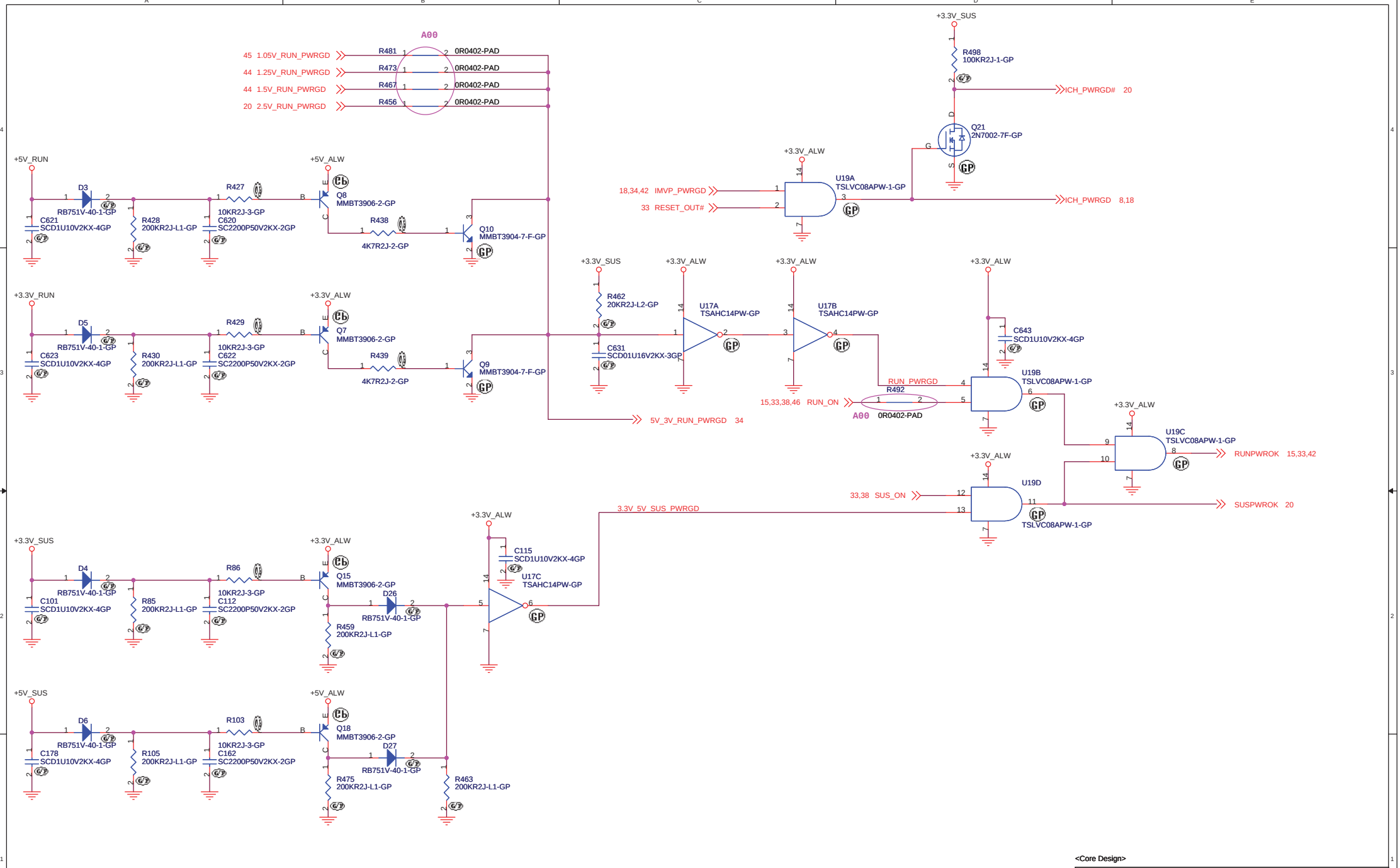

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power On Logic***

Size	Document Number	Rev
A3	**Siberia**	**A00**

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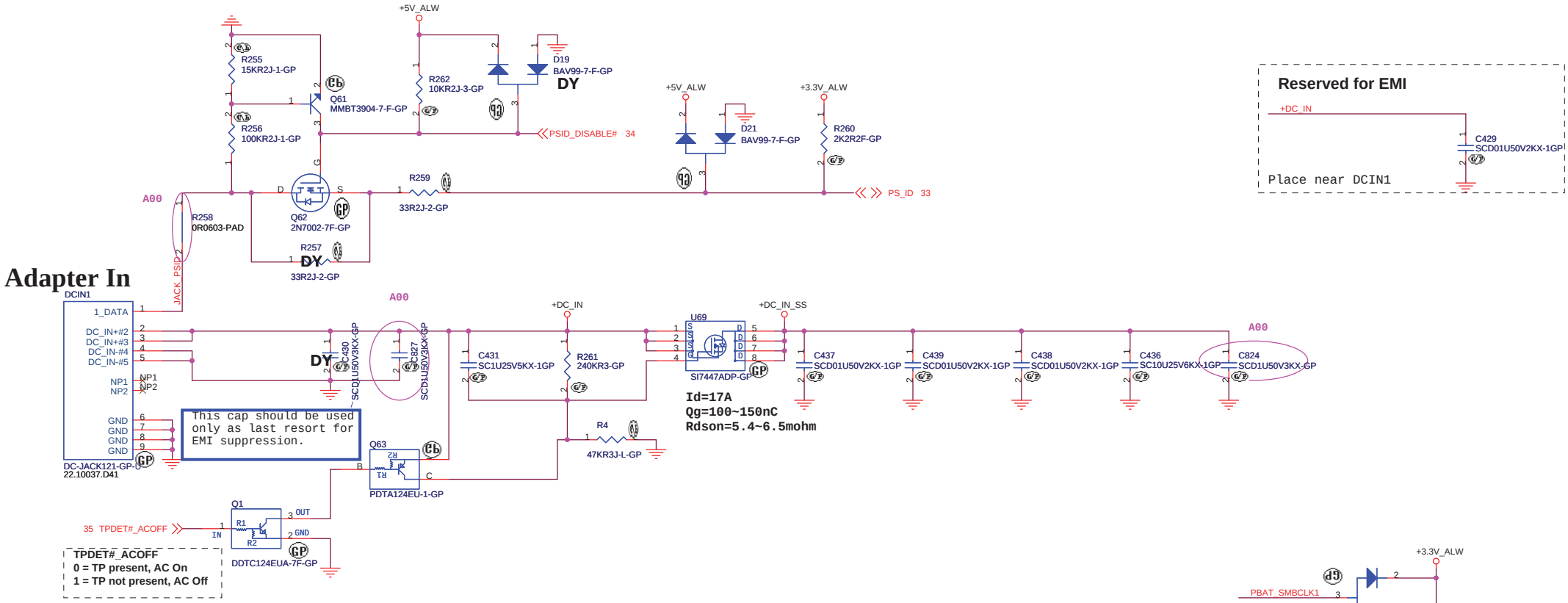
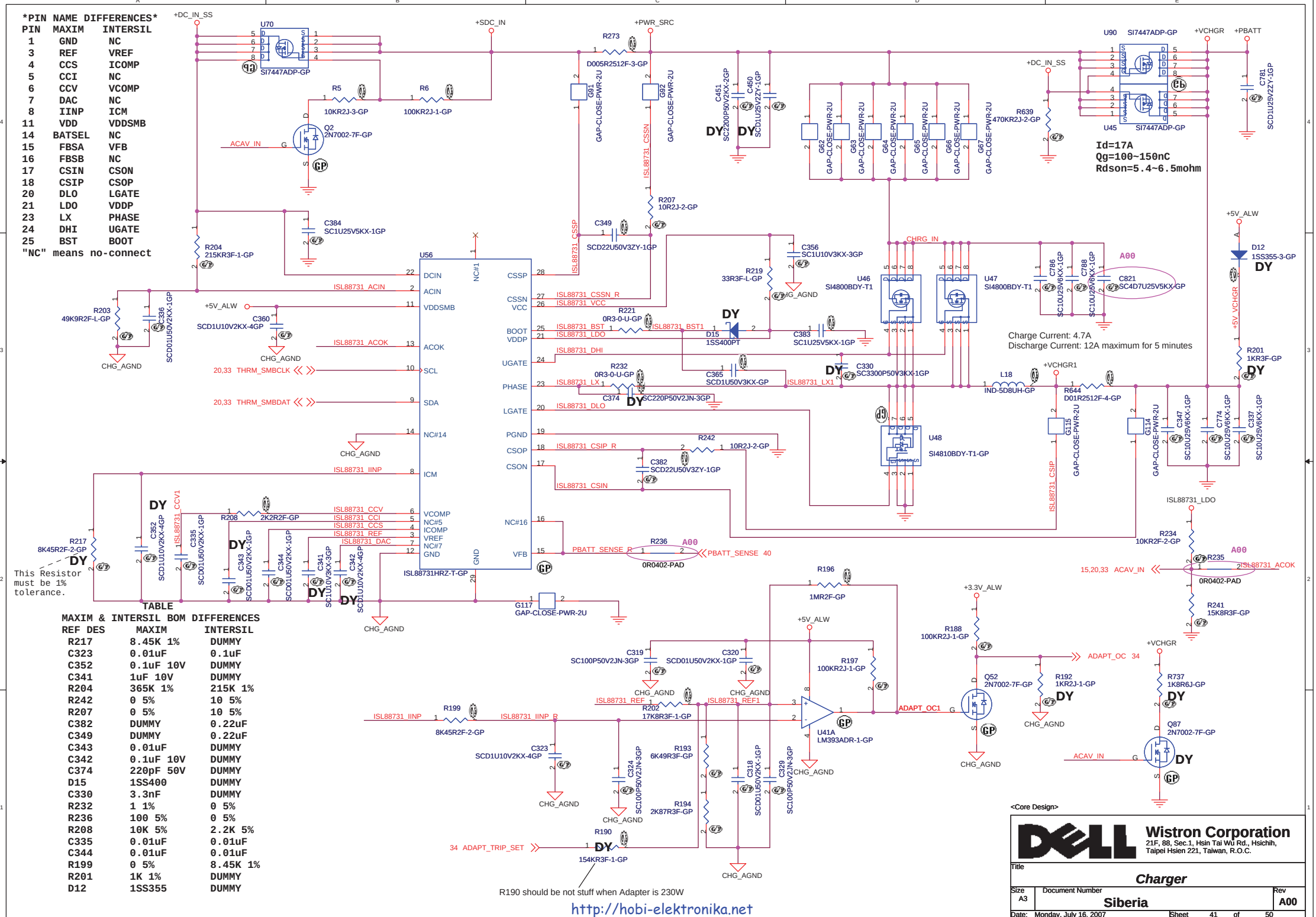


http://hobi-elektronika.net


PIN NAME DIFFERENCES
PIN MAXIM INTERSIL
1 GND NC
3 REF VREF
4 CCS ICOMP
5 CCI NC
6 CCV VCOMP
7 DAC NC
8 IINP ICM
11 VDD VDDSMB
14 BATSEL NC
15 FBSA VFB
16 FBSB NC
17 CSIN CSON
18 CSIP CSOP
20 DLO LGATE
21 LDO VDDP
23 LX PHASE
24 DHI UGATE
25 BST BOOT
"NC" means no-connect
U56
ISL88731HRZ-T-GP
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
ICM
VCOMP
NC#5
ICOMP
VREF
NC#7
GND
CSSP
CSSN
VCC
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
U70 SI7447ADP-GP
U90 SI7447ADP-GP
U45 SI7447ADP-GP
Id=17A
Qg=100~150nC
Rdson=5.4~6.5mohm
U46 SI4800BDY-T1
U47 SI4800BDY-T1
U48 SI4810BDY-T1-GP
Charge Current: 4.7A
Discharge Current: 12A maximum for 5 minutes
This Resistor must be 1% tolerance.
TABLE
MAXIM & INTERSIL BOM DIFFERENCES
REF DES MAXIM INTERSIL
R217 8.45K 1% DUMMY
C323 0.01uF 0.1uF
C352 0.1uF 10V DUMMY
C341 1uF 10V DUMMY
R204 365K 1% 215K 1%
R242 0 5% 10 5%
R207 0 5% 10 5%
C382 DUMMY 0.22uF
C349 DUMMY 0.22uF
C343 0.01uF DUMMY
C342 0.1uF 10V DUMMY
C374 220pF 50V DUMMY
D15 1SS400 DUMMY
C330 3.3nF DUMMY
R232 1 1% 0 5%
R236 100 5% 0 5%
R208 10K 5% 2.2K 5%
C335 0.01uF 0.01uF
C344 0.01uF 0.01uF
R199 0 5% 8.45K 1%
R201 1K 1% DUMMY
D12 1SS355 DUMMY
R190 should be not stuff when Adapter is 230W
http://hobi-elektronika.net
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
Charger
Size A3
Document Number
Siberia
Rev A00
Date: Monday, July 16, 2007
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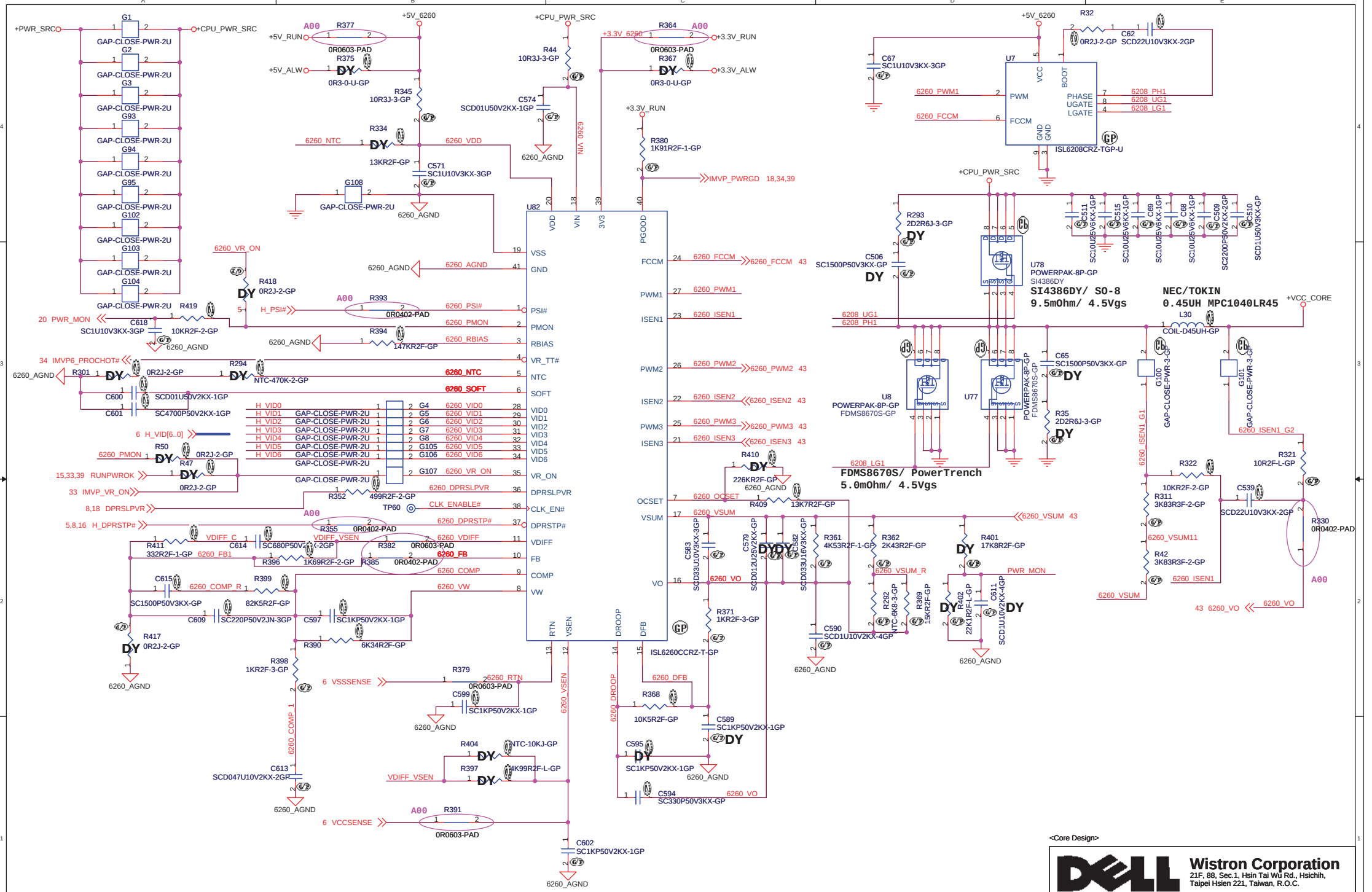
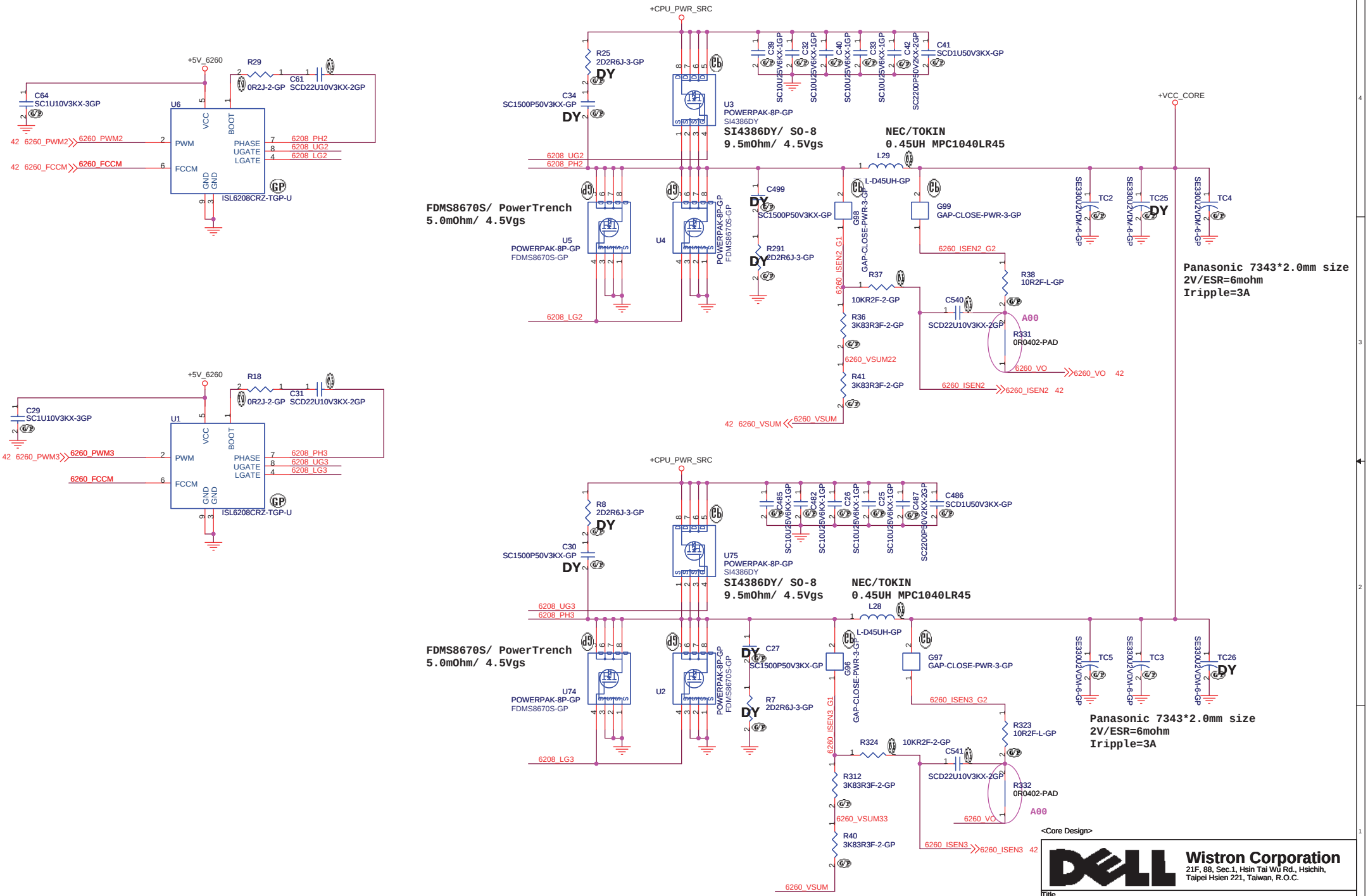

U82
ISL6260CCRZ-T-GP
U7
ISL6208CRZ-TGP-U
U78
POWERPAK-8P-GP
SI4386DY
SI4386DY/ SO-8
9.5mOhm/ 4.5Vgs
NEC/TOKIN
0.45UH MPC1040LR45
U8
POWERPAK-8P-GP
FDMS8670S-GP
U77
FDMS8670S/ PowerTrench
5.0mOhm/ 4.5Vgs
+PWR_SRC
+CPU_PWR_SRC
+5V_6260
+5V_RUN
+5V_ALW
+3.3V_6260
+3.3V_RUN
+3.3V_ALW
+VCC_CORE
IMVP_PWRGD 18,34,39
6260_FCCM 43
6260_PWM2 43
6260_ISEN2 43
6260_PWM3 43
6260_ISEN3 43
6260_VSUM 43
43 6260_VO
6260_AGND
6260_VR_ON
6260_PSI#
6260_PMON
6260_RBIAS
6260_NTC
6260_SOFT
6260_VID0
6260_VID1
6260_VID2
6260_VID3
6260_VID4
6260_VID5
6260_VID6
6260_VR_ON
6260_DPRSLPVR
CLK_ENABLE#
6260_DPRSTP#
6260_VDIFF
6260_FB
6260_COMP
6260_VW
6260_RTN
6260_VSEN
6260_DROOP
6260_DFB
6260_OCSET
6260_VSUM
6260_VO
6260_PWM1
6260_ISEN1
6208_PH1
6208_UG1
6208_LG1
6260_PWM1
6260_FCCM
6260_ISEN1_G2
6260_VSUM11
6260_VSUM_R
6260_ISEN1
PWR_MON
6260_VSUM
6260_VO
6260_COMP_R
6260_FB1
6260_COMP 1
VDIFF_VSEN
6 VSSSENSE
6 VCCSENSE
6 H_VID[6..0]
20 PWR_MON
34 IMVP6_PROCHOT#
15,33,39 RUNPWROK
33 IMVP_VR_ON
8,18 DPRSLPVR
5,8,16 H_DPRSTP#
NIA 0929
A00
DY
GP
http://hobi-elektronika.net
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU Vcore Power_1
Size A3
Document Number
Siberia
Rev A00
Date: Monday, July 16, 2007
Sheet 42 of 50



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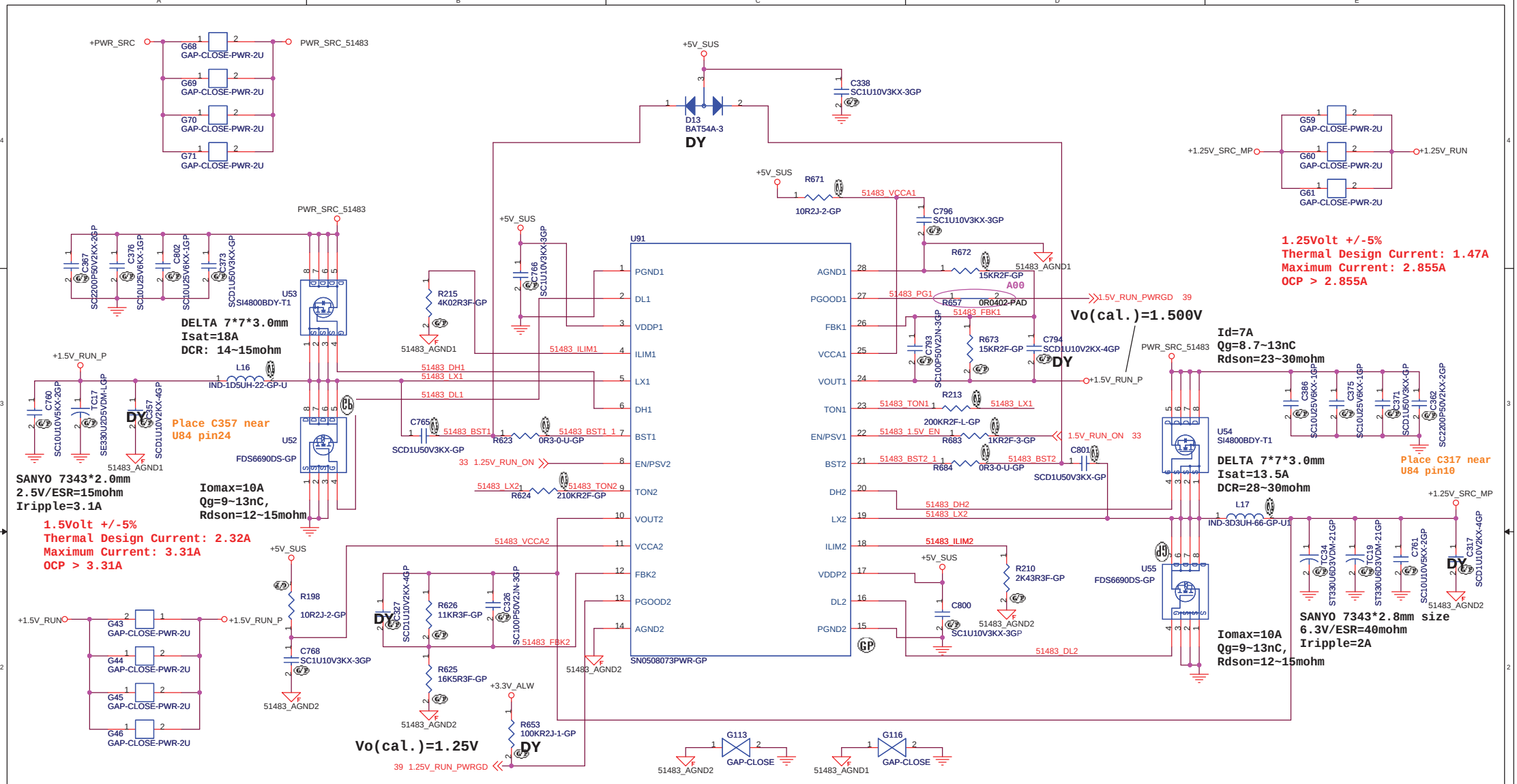

Vtrip(mV)=Rtrip(Kohm)*10(uA)
Iocp=(Vtrip/Rdson)+((1/2*L*f)*((Vin-Vout)*Vou)/Vin
Vout=(1+(Rtop/Rbottom))*0.75

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DC to DC 1.5V/ 1.25V

Size: A3 | Document Number: Siberia | Rev: A00

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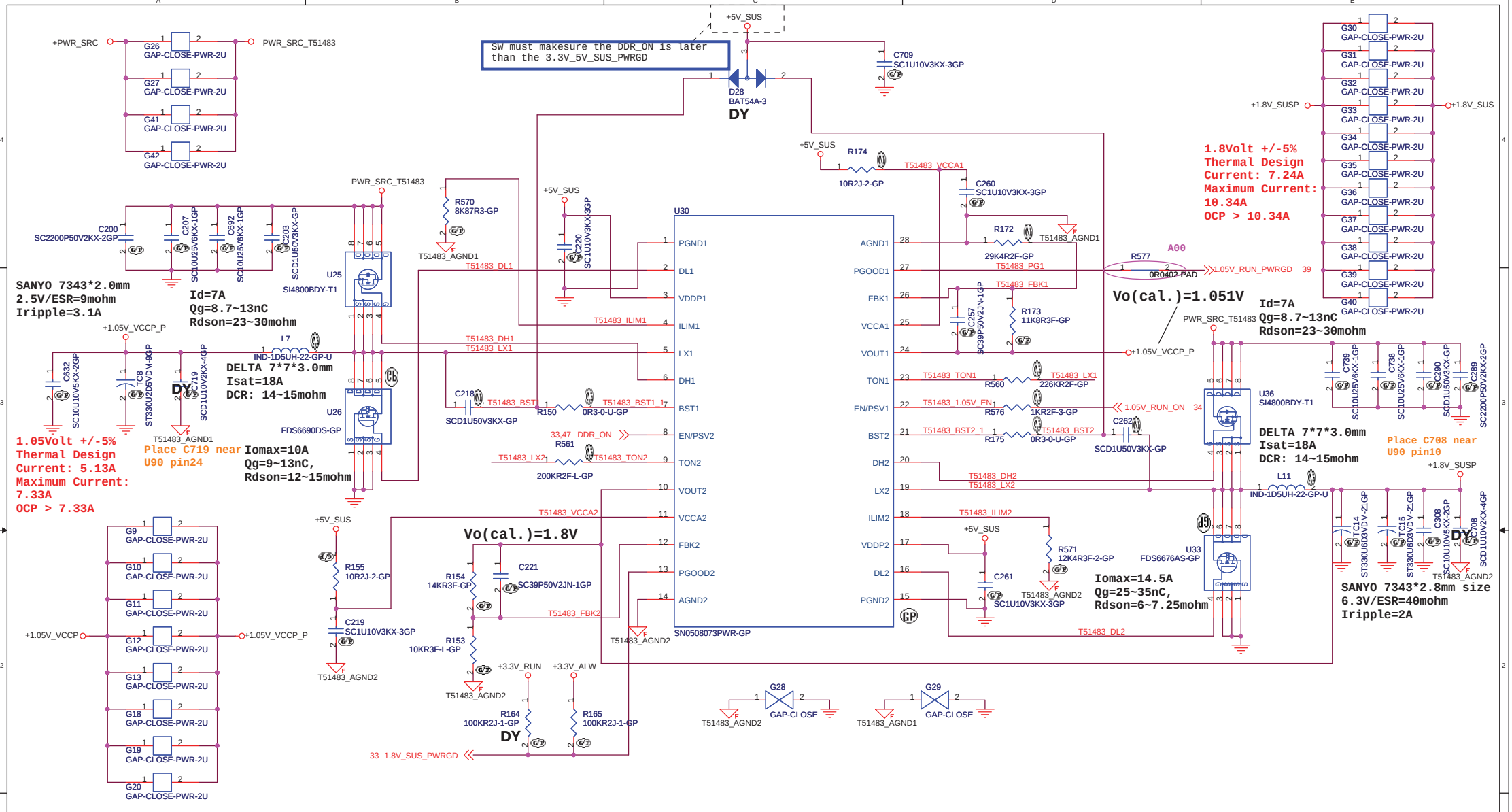
SW must makesure the DDR_ON is later than the 3.3V_5V_SUS_PWRGD
+5V_SUS
D28
BAT54A-3
DY
C709
SC1U10V3KX-3GP
+PWR_SRC
PWR_SRC_T51483
G26 GAP-CLOSE-PWR-2U
G27 GAP-CLOSE-PWR-2U
G41 GAP-CLOSE-PWR-2U
G42 GAP-CLOSE-PWR-2U
G30 GAP-CLOSE-PWR-2U
G31 GAP-CLOSE-PWR-2U
G32 GAP-CLOSE-PWR-2U
G33 GAP-CLOSE-PWR-2U
G34 GAP-CLOSE-PWR-2U
G35 GAP-CLOSE-PWR-2U
G36 GAP-CLOSE-PWR-2U
G37 GAP-CLOSE-PWR-2U
G38 GAP-CLOSE-PWR-2U
G39 GAP-CLOSE-PWR-2U
G40 GAP-CLOSE-PWR-2U
+1.8V_SUSP
+1.8V_SUS
1.8Volt +/-5%
Thermal Design
Current: 7.24A
Maximum Current:
10.34A
OCP > 10.34A
R174
10R2J-2-GP
T51483_VCCA1
C260
SC1U10V3KX-3GP
R172
29K4R2F-GP
T51483_AGND1
R577
0R0402-PAD
A00
1.05V_RUN_PWRGD 39
Vo(cal.)=1.051V
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
PWR_SRC_T51483
C200
SC2200P50V2KX-2GP
C207
SC10U25V6KX-1GP
C692
SC10U25V6KX-1GP
C203
SCD1U50V3KX-GP
U25
SI4800BDY-T1
SANYO 7343*2.0mm
2.5V/ESR=9mohm
Iripple=3.1A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
R570
8K87R3-GP
T51483_AGND1
T51483_DL1
C220
SC1U10V3KX-3GP
U30
PGND1
DL1
VDDP1
ILIM1
LX1
DH1
BST1
EN/PSV2
TON2
VOUT2
VCCA2
FBK2
PGOOD2
AGND2
AGND1
PGOOD1
FBK1
VCCA1
VOUT1
TON1
EN/PSV1
BST2
DH2
LX2
ILIM2
VDDP2
DL2
PGND2
SN0508073PWR-GP
T51483_ILIM1
T51483_DH1
T51483_LX1
T51483_PG1
T51483_FBK1
C257
SC39P50V2JN-1GP
R173
11K8R3F-GP
+1.05V_VCCP_P
+1.05V_VCCP_P
L7
IND-1D5UH-22-GP-U
DELTA 7*7*3.0mm
Isat=18A
DCR: 14~15mohm
C632
SC10U10V5KX-2GP
C628
ST330U2D5VDM-9GP
C719
SCD1U10V2KX-4GP
DY
U26
FDS6690DS-GP
T51483_AGND1
1.05Volt +/-5%
Thermal Design
Current: 5.13A
Maximum Current:
7.33A
OCP > 7.33A
Place C719 near
U90 pin24
Iomax=10A
Qg=9~13nC,
Rdson=12~15mohm
C218
SCD1U50V3KX-GP
T51483_BST1
R150
0R3-0-U-GP
33,47 DDR_ON
R561
200KR2F-L-GP
T51483_LX2
T51483_TON2
T51483_TON1
R560
226KR2F-GP
T51483_LX1
T51483_1.05V_EN
R576
1KR2F-3-GP
1.05V_RUN_ON 34
T51483_BST2_1
R175
0R3-0-U-GP
T51483_BST2
C262
SCD1U50V3KX-GP
T51483_DH2
T51483_LX2
T51483_ILIM2
R571
12K4R3F-2-GP
T51483_AGND2
C261
SC1U10V3KX-3GP
T51483_DL2
U33
FDS6676AS-GP
Iomax=14.5A
Qg=25~35nC,
Rdson=6~7.25mohm
U36
SI4800BDY-T1
DELTA 7*7*3.0mm
Isat=18A
DCR: 14~15mohm
C739
SC10U25V6KX-1GP
C738
SC10U25V6KX-1GP
C290
SCD1U50V3KX-GP
C289
SC2200P50V2KX-2GP
Place C708 near
U90 pin10
+1.8V_SUSP
L11
IND-1D5UH-22-GP-U
TC14
ST330U6D3VDM-21GP
TC15
ST330U6D3VDM-21GP
C308
SC10U10V5KX-2GP
C708
SCD1U10V2KX-4GP
DY
T51483_AGND2
SANYO 7343*2.8mm size
6.3V/ESR=40mohm
Iripple=2A
G9 GAP-CLOSE-PWR-2U
G10 GAP-CLOSE-PWR-2U
G11 GAP-CLOSE-PWR-2U
G12 GAP-CLOSE-PWR-2U
G13 GAP-CLOSE-PWR-2U
G18 GAP-CLOSE-PWR-2U
G19 GAP-CLOSE-PWR-2U
G20 GAP-CLOSE-PWR-2U
+1.05V_VCCP
+1.05V_VCCP_P
+5V_SUS
R155
10R2J-2-GP
C219
SC1U10V3KX-3GP
T51483_AGND2
Vo(cal.)=1.8V
R154
14KR3F-GP
C221
SC39P50V2JN-1GP
T51483_FBK2
R153
10KR3F-L-GP
T51483_AGND2
+3.3V_RUN
+3.3V_ALW
R164
100KR2J-1-GP
DY
R165
100KR2J-1-GP
33 1.8V_SUS_PWRGD
G28
GAP-CLOSE
T51483_AGND2
G29
GAP-CLOSE
T51483_AGND1
Vtrip(mV)=Rtrip(Kohm)*10(uA)
Iocp=(Vtrip/Rdson)+((1/2*L*f)*((Vin-Vout)*Vou)/Vin
Vout=(1+(Rtop/Rbottom))*0.75
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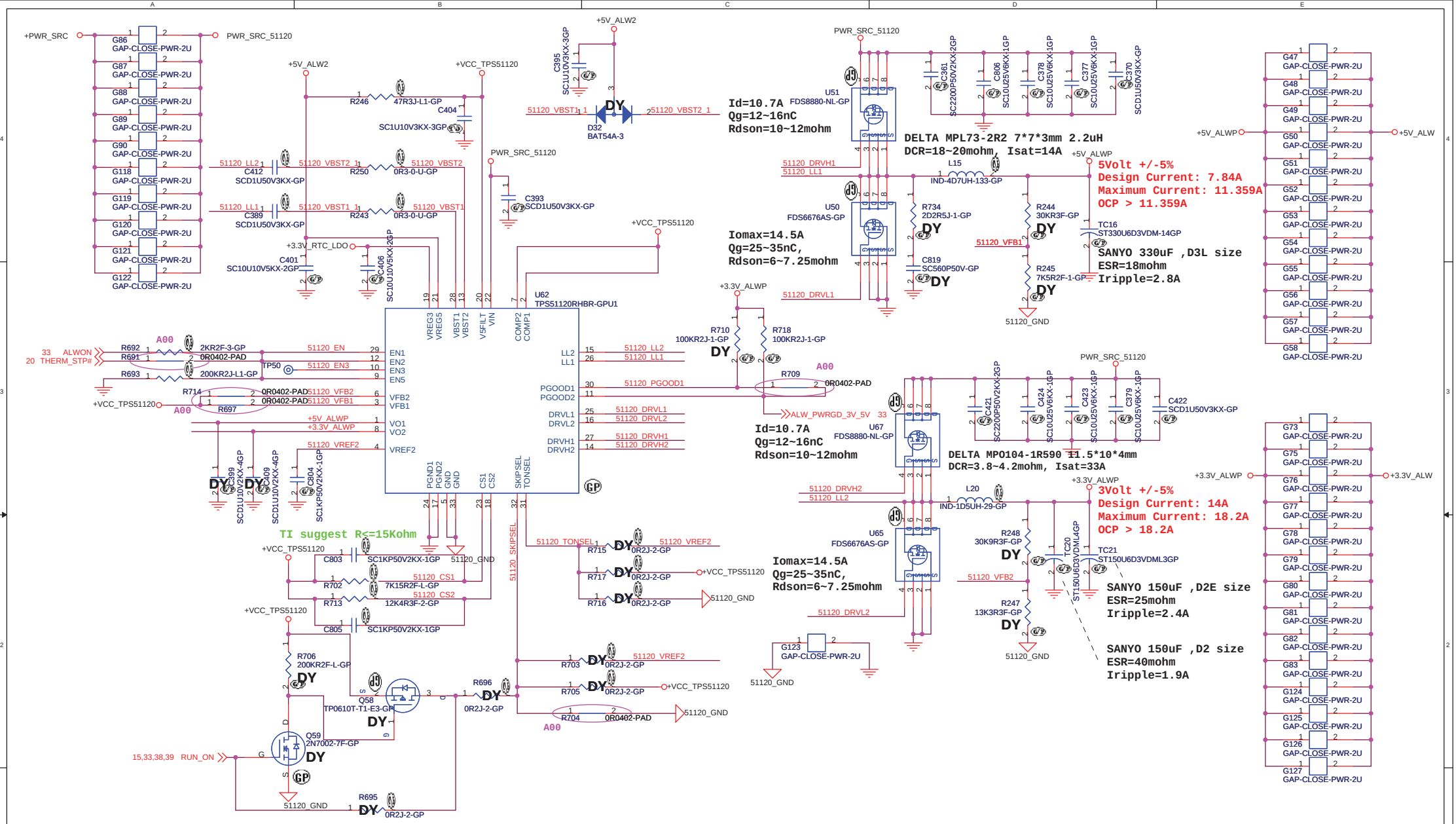
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DC to DC 1.8V/ 1.05V
Size A3
Document Number
Siberia
Rev A00
Date: Monday, July 16, 2007
Sheet 45 of 50



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 580k/CH2	**280k/CH1 430k/CH2**	220k/CH1 330k/CH2	180k/CH1 2870k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	Swithchr ON	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

Vout=1V*(R1+R2)/R2

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<Core Design>

Wistron Corporation
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Title: *DC to DC 3.3V / 5V*

Size: A3 | Document Number: **Siberia** | Rev: **A00**

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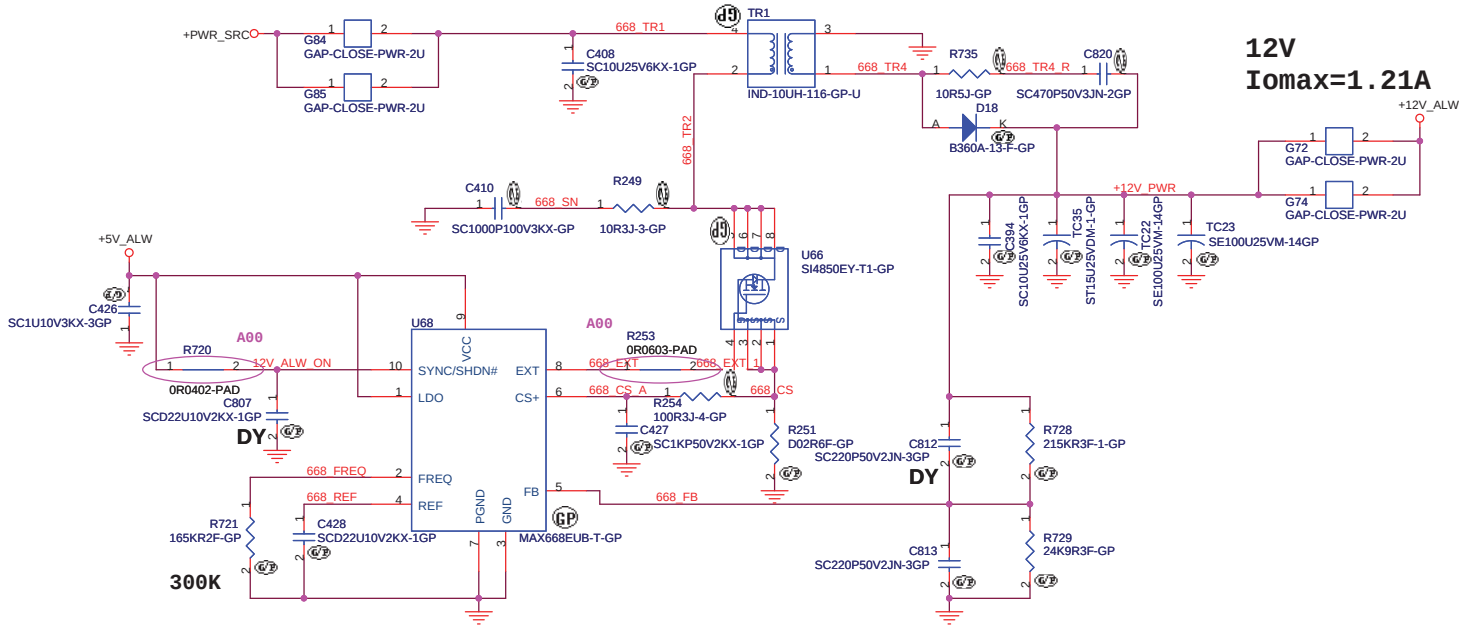

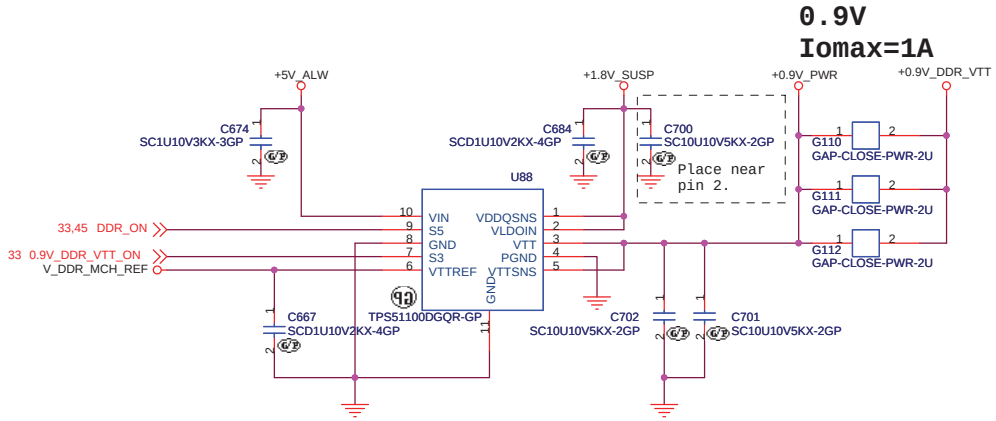

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ***DC to DC 12V / 0.9V***

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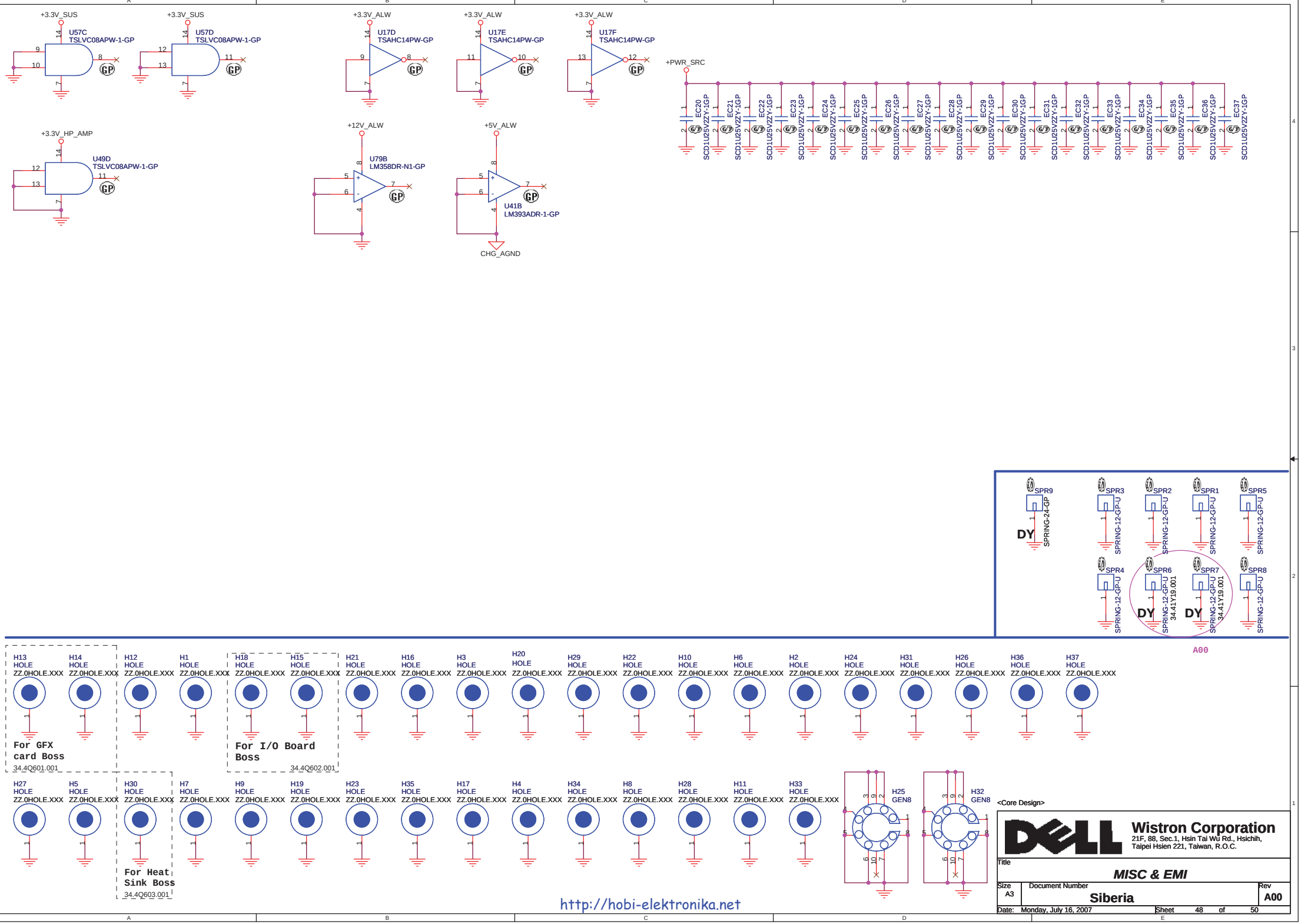
+3.3V_SUS
U57C
TSLVC08APW-1-GP
+3.3V_SUS
U57D
TSLVC08APW-1-GP
+3.3V_ALW
U17D
TSAHC14PW-GP
+3.3V_ALW
U17E
TSAHC14PW-GP
+3.3V_ALW
U17F
TSAHC14PW-GP
+PWR_SRC
EC20 SCD1U25V2ZY-1GP
EC21 SCD1U25V2ZY-1GP
EC22 SCD1U25V2ZY-1GP
EC23 SCD1U25V2ZY-1GP
EC24 SCD1U25V2ZY-1GP
EC25 SCD1U25V2ZY-1GP
EC26 SCD1U25V2ZY-1GP
EC27 SCD1U25V2ZY-1GP
EC28 SCD1U25V2ZY-1GP
EC29 SCD1U25V2ZY-1GP
EC30 SCD1U25V2ZY-1GP
EC31 SCD1U25V2ZY-1GP
EC32 SCD1U25V2ZY-1GP
EC33 SCD1U25V2ZY-1GP
EC34 SCD1U25V2ZY-1GP
EC35 SCD1U25V2ZY-1GP
EC36 SCD1U25V2ZY-1GP
EC37 SCD1U25V2ZY-1GP
+3.3V_HP_AMP
U49D
TSLVC08APW-1-GP
+12V_ALW
U79B
LM358DR-N1-GP
+5V_ALW
U41B
LM393ADR-1-GP
CHG_AGND
SPR9 SPRING-24-GP
DY
SPR3 SPRING-12-GP-U
SPR2 SPRING-12-GP-U
SPR1 SPRING-12-GP-U
SPR5 SPRING-12-GP-U
SPR4 SPRING-12-GP-U
SPR6 SPRING-12-GP-U 34.41Y19.001
SPR7 SPRING-12-GP-U 34.41Y19.001
SPR8 SPRING-12-GP-U
DY
DY
A00
H13 HOLE ZZ.0HOLE.XXX
H14 HOLE ZZ.0HOLE.XXX
H12 HOLE ZZ.0HOLE.XXX
H1 HOLE ZZ.0HOLE.XXX
H18 HOLE ZZ.0HOLE.XXX
H15 HOLE ZZ.0HOLE.XXX
H21 HOLE ZZ.0HOLE.XXX
H16 HOLE ZZ.0HOLE.XXX
H3 HOLE ZZ.0HOLE.XXX
H20 HOLE ZZ.0HOLE.XXX
H29 HOLE ZZ.0HOLE.XXX
H22 HOLE ZZ.0HOLE.XXX
H10 HOLE ZZ.0HOLE.XXX
H6 HOLE ZZ.0HOLE.XXX
H2 HOLE ZZ.0HOLE.XXX
H24 HOLE ZZ.0HOLE.XXX
H31 HOLE ZZ.0HOLE.XXX
H26 HOLE ZZ.0HOLE.XXX
H36 HOLE ZZ.0HOLE.XXX
H37 HOLE ZZ.0HOLE.XXX
For GFX card Boss
34.4Q601.001
For I/O Board Boss
34.4Q602.001
H27 HOLE ZZ.0HOLE.XXX
H5 HOLE ZZ.0HOLE.XXX
H30 HOLE ZZ.0HOLE.XXX
H7 HOLE ZZ.0HOLE.XXX
H9 HOLE ZZ.0HOLE.XXX
H19 HOLE ZZ.0HOLE.XXX
H23 HOLE ZZ.0HOLE.XXX
H35 HOLE ZZ.0HOLE.XXX
H17 HOLE ZZ.0HOLE.XXX
H4 HOLE ZZ.0HOLE.XXX
H34 HOLE ZZ.0HOLE.XXX
H8 HOLE ZZ.0HOLE.XXX
H28 HOLE ZZ.0HOLE.XXX
H11 HOLE ZZ.0HOLE.XXX
H33 HOLE ZZ.0HOLE.XXX
For Heat Sink Boss
34.4Q603.001
H25 GEN8
H32 GEN8
http://hobi-elektronika.net
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
MISC & EMI
Size A3
Document Number
Siberia
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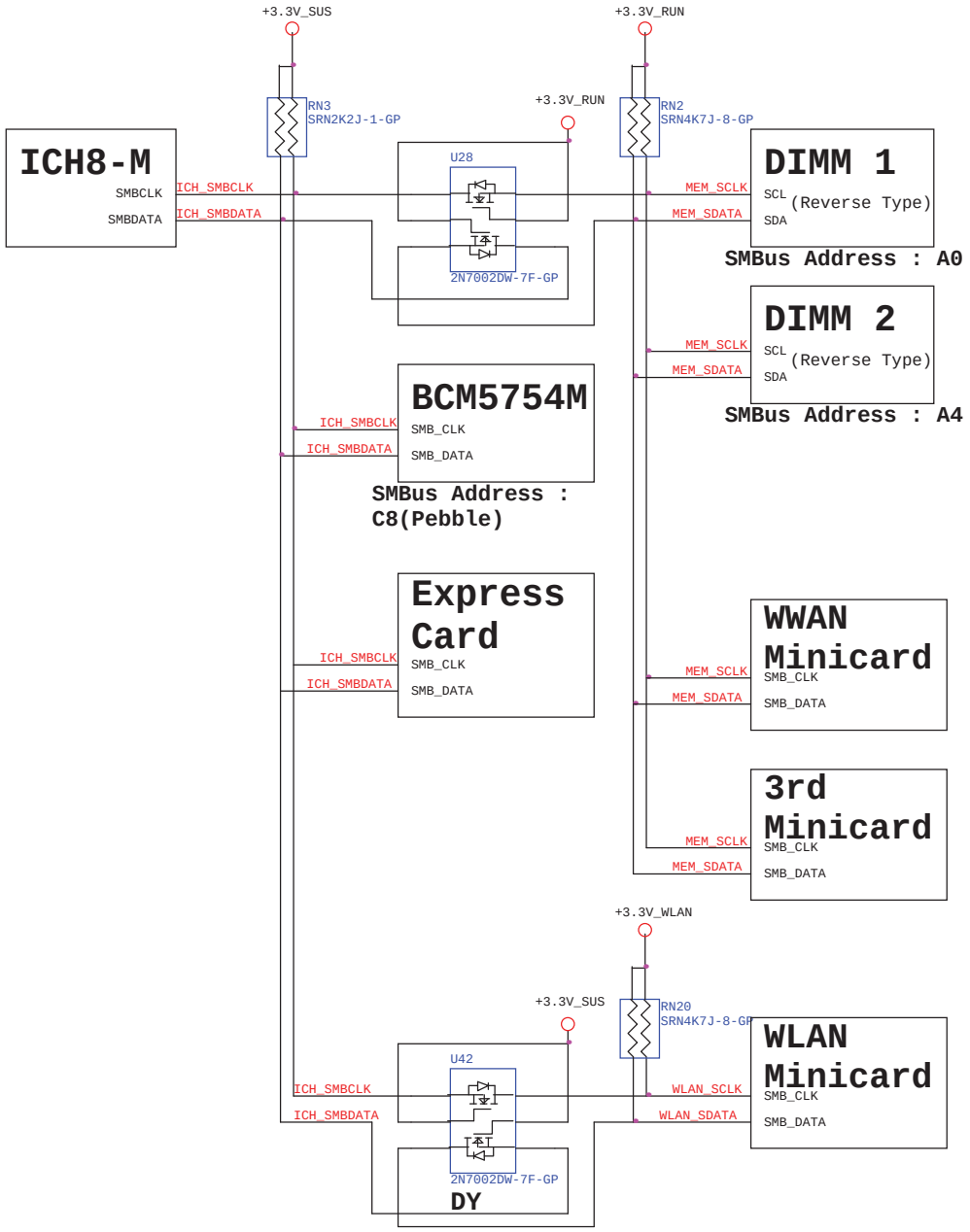
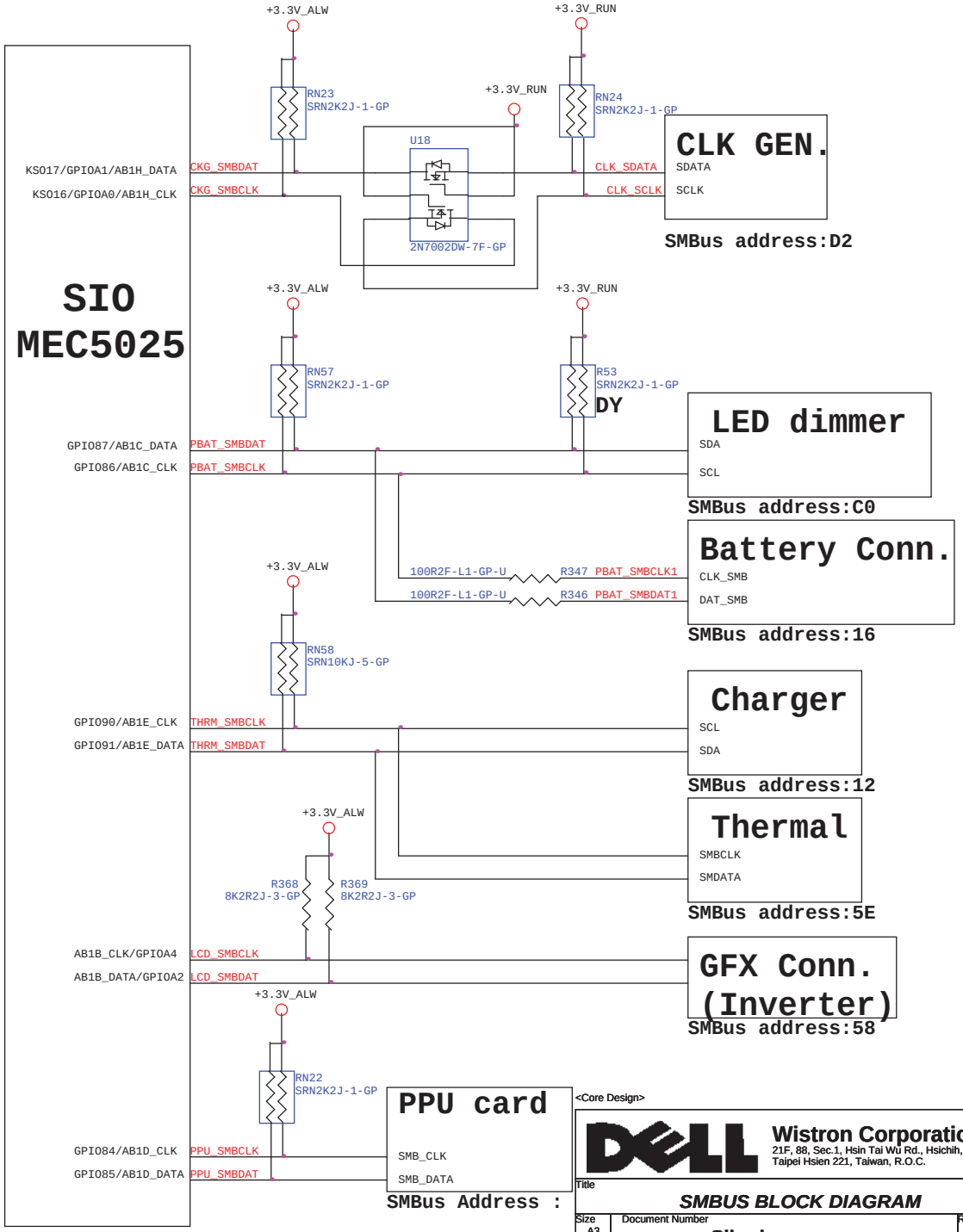
Date: Monday, July 16, 2007
Sheet 48 of 50

ICH8 SMBus Block Diagram



KBC SMBus Block Diagram



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<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SMBUS BLOCK DIAGRAM

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Date: Monday, July 16, 2007 Sheet 49 of 50

DATE	VERSON	ITEM	PAGE	Modify List	Issue Description	OWNER
2007/07/12	X02 to A00	1	19	Change C245 from 0.1U 0402 size to 1U 0603 size. (BITs ID:SCH159348)	Dell's command for ICH8 VREF power sequence glitch.	EE
		2	34	Populate R407 and non-populate R388.	Change board ID from X02 to A00.	EE
		3	36	Change U16 to vendor MXIC.	Because SST have shortage issue.	EE
		4	48	Non-populate SPR6, SPR7.(BITs ID:SCH159349)	Can't touch case.	EE
		5	4	Populate C661, C694 to 10p 50V 0402 size. Populate C693 to 8.2p 50V 0402 size.	Solution for 33MHz EMI issue.	EE
		6	4	Purge ICS CLK gen. and put Cypress at main source.	ICS CLK gen. has warn boot issue.	EE
		7	24	Add R739 10K ohm pull-high to +3.3V_RUN.(SCH159171)	For audio AUD_EAPD#.	EE
		8	41	Remove C354 and C358, add C821 as 4.7U 25V 0805.		EMI
		9	15	Add C823 as 0.1U 50V 0603 for +GFX_PWR_SRC.		EMI
		10	40	Add C827 as 0.1U 50V 0603 for +DC_IN.		EMI
		11	40	Add C824 as 0.1U 50V 0603 for +DC_IN_SS.		EMI
		12	40	Add C826 as 0.1uF for +PBATT. Change R218 to close gap.		EMI
		13	28	Populate C434 and C435 as 47pF, non-populate R265. Change L21 to 2500ohm bead.		EMI
		14	27	Change R285 from 1.24K ohm 5% to 1.27K ohm 1%. Change C449 and C461 to 47pF, C447 to 4.7uF.		EMI
		15	31	Non-pop R588, R590.	Command from DELL wireless team.	EE
		16		Change many 0ohm resistors to wire pad.		EE

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